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elektor

up-to-date electronics for lab and leisure

elektor piano

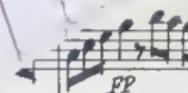
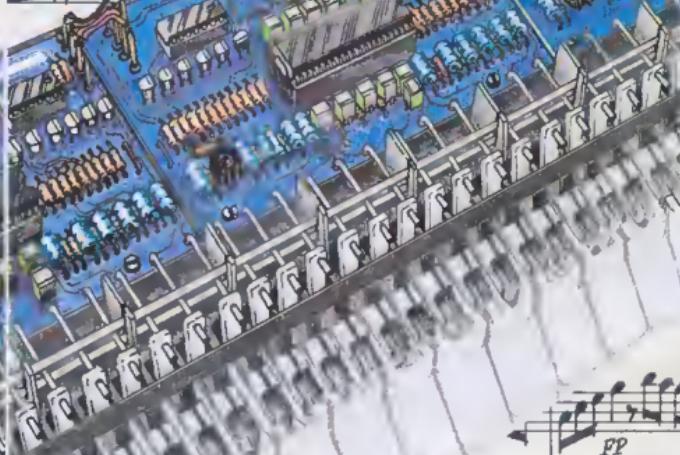


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hot news!

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The MK14 can be assembled by anyone with a fine-tip soldering iron and a few hours spare time, using the illustrated step-by-step instructions provided.

Tomorrow's technology - today!

It is not unreasonable to assume that within the next five years there will be hardly any companies engaged in electronics that are not using microprocessors in one area or another.

Phil Pittman, Wireless World, Nov 1977

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What is a TUN?

What is 10 n?

What is the EPS service?

What is the TO service?

What is a missing link?

Semiconductor types

Very often, a large number of equivalent semiconductors exist with different type numbers. For this reason, 'abbreviated' type numbers are used in Elektor wherever possible.

a '747' stand for μ p741,
LM741, MC741, M741,
RM741, SN72741, etc.

a 'TUP' or 'TUN' (Transistor, Universal, PNP or NPN respectively) stand for any low frequency silicon transistor that meets the following specifications.

UCEO, max	20V
IC, max	100 mA
hFE, min	100
Ptot, max	100 mW
ft, min	100 MHz

Some 'TUN's are BC107, BC108 and BC109 families, 2N3856A, 2N3857, 2N3860, 2N3904, 2N3947, 2N4124. Some 'TUP's are BC177 and BC178 families, BC179 family with the possible exception of BC159 and BC179; 2N2412, 2N3251, 2N3906, 2N4126, 2N4291.

a 'DUS' or 'DUG' (Diode Universal, Silicon or Germanium respectively) stands for any diode that meets the following specifications

	DUS	DUG
UZ, max	25V	20V
IF, max	100mA	35mA
IR, max	1μA	100 μA
Ptot, max	250mW	.250mW
CD, max	5pF	10pF

Some 'DUS's are: BA127, BA217, BA218, BA221, BA222, BA317, BA318, BA313, BA314, BA315, BA316, BA317, BA318, BA319, AA116.

a 'BC107B', 'BC237B', 'BC547B' all refer to the same 'family' of almost identical better-quality silicon transistors. In general, any other member of the same family can be used instead.

BC107 (B, -9) families

BC107 (B, -9), BC147 (B, -9), BC207 (B, -9), BC237 (B, -9), BC317 (B, -9), BC347 (B, -9), BC547 (B, -9), BC171 (B, -2, -3), BC182 (B, -3), BC382 (B, -3), BC437 (B, -9), BC414

BC177 (B, -9) families

BC177 (B, -9), BC157 (B, -9), BC204 (B, -5), BC307 (B, -9), BC320 (B, -1), BC350 (B, -1, 2), BC557 (B, -9), BC251 (B, -2, -3), BC212 (B, -3), BC512 (B, -3, 4), BC261 (B, -2, -3), BC416

Resistor and capacitor values

When giving component values, decimal points and large numbers

1 of zeros are avoided wherever possible. The decimal point is usually replaced by one of the following abbreviations

p (pico-) = 10^{-12}

n (nano-) = 10^{-9}

μ (micro-) = 10^{-6}

m (milli-) = 10^{-3}

k (kilo-) = 10^3

M (mega-) = 10^6

G (giga-) = 10^9

A few examples

Resistance value 2k7 2700 Ω.

Resistance value 470, 470 Ω.

Capacitance value 4p7 4.7 pF, or

0.000 000 004 7 F.

Capacitance value 10n this is the international way of writing

10,000 pF or 01 μF, since 1 n is 10^{-9} farad or 1000 pF.

Resistors are 1 Watt 5% carbon types, unless otherwise specified.

The DC working voltage of

capacitors (other than electrolytics) is normally assumed to be

at least 60 V. As a rule of thumb, a safe value is usually approximately twice the DC supply voltage

Test voltages

The DC test voltages shown are measured with a 20 kΩ/V instrument, unless otherwise specified. U, not V

The international letter symbol 'U' for voltage is often used instead of the ambiguous 'V'. 'V' is normally reserved for 'volts'. For instance, $U_B = 10$ V, not $V_B = 10$ V.

Mains voltages

No mains (power line) voltages are listed in Elektor circuits. It is assumed that our readers know what voltage is standard in their part of the world!

Readers in countries that use 60 Hz should note that Elektor circuits are designed for 50 Hz operation. This will not normally be a problem, however, in cases where the mains frequency is used for synchronisation some modification may be required.

Technical services to readers a EPS service: Many Elektor articles include a lay-out for a printed circuit board. Some - but not all - of these boards are available ready-etched and predrilled. The 'EPS print service list' in the current issue always gives a complete list of available boards.

a Technical queries: Members of the technical staff are available to answer technical queries (relating to articles published in Elektor) by telephone on Mondays from 14.00 to 16.30. Letters with technical queries should be addressed to: Dept. TQ. Please enclose a stamped, self addressed envelope, readers outside U.K. please enclose an IRC instead of stamps.

a Missing link: Any important modifications to, additions to, improvements on or corrections in Elektor circuits are generally listed under the heading 'Missing Link' at the earliest opportunity.

The puffometer, whilst making no claims to providing accurate measurements, however does represent a relatively simple (and amusing) means of measuring just how long-winded some people are. It's great for parties!

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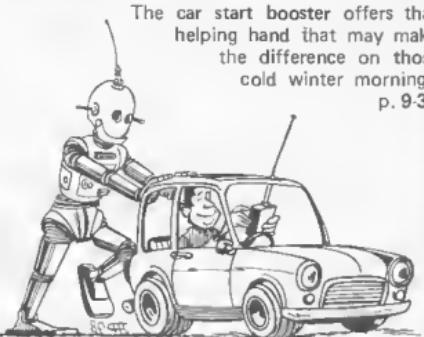
Electronic temperature-controlled soldering irons offer many advantages over the continuous heat types. The Elektor circuit is a thermostatic control unit, which is both easy to build and uses standard parts.

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The car start booster offers that helping hand that may make the difference on those cold winter mornings.

p. 9-30



An artist's impression of the Elektor piano, which may not replace the Steinway but does have many applications where cost and portability are important factors.



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buffered/unbuffered CMOS	9-43
Many CMOS digital ICs are now available in two versions, buffered and unbuffered. The lack of information available to the amateur on the differences between them has given rise to some confusion as to the compatibility of the two types. This article examines both types of CMOS and compares them with TTL.	
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selektor

Blue Fox

Blue Fox is an integral part of the weapons system of the Royal Navy's Sea Harrier vertical take off fighter/strike/reconnaissance aircraft.

A distinctive feature of the radar is its flat aperture aerial designed to increase detection range and produce minimum sidelobes. Another distinctive feature is that the scanner is stabilised in both pitch and roll. Roll stabilisation assists in achieving the maximum accuracy in air-to-surface attacks.

Blue Fox is a lightweight radar weighing less than 190 lbs (86 kgs). It is designed to fulfill a dual role: that of airborne search and interception; and air-to-surface search-and-strike.

Having successfully completed its initial ground trials, Blue Fox is currently being prepared for flight trials later this year (1978).

Blue Fox is a monopulse radar operating in the X-band. Frequency agility maximises its ability to detect small targets in clutter conditions and also improves its immunity to electronic countermeasures.

For air-to-air interceptions Blue Fox provides directional and range data to the Sea Harrier's weapon-aiming

computer for lead-pursuit or chase attacks. In the strike role it will be used for aiming air-to-surface weapons, the radar derived information providing weapon-release data.

Blue Fox employs monopulse techniques in both the horizontal and vertical planes. When searching for distant targets a PPI scan can be used and changed to a sector B scan if required. The pilot may choose either a single-bar or multiple-bar search scan pattern depending on the amount of sky to be covered.

The main radar unit comprises a number of line replaceable units (LRUs). Built-in test facilities are provided to enable faulty LRUs to be identified and replaced at the first-line servicing level. Modular construction and detail design simplify the replacement of any unserviceable components at second and third-line maintenance levels. Predicted meantime between mission failures is in excess of 120 hours.

Because Blue Fox is designed for a relatively small aircraft, is of modular construction, and light in weight, it is expected to prove suitable for installation in many other types of aircraft and, as such, possesses considerable development potential.

*Electronic Systems Department,
Ferranti Limited, Ferry Road,
Edinburgh, EH5 2XS, England*

(347 S)

Unmanned submersible

A completely new type of micro-computer-controlled unmanned inspection system - built to operate in the poor visibility and hostile operating conditions of the North Sea - has been

launched by Richmond-based Marine Unit Technology Limited. The new vehicle - which is supported by the Department of Energy through the offshore Energy Technology Board - is lighter, smaller, more versatile, and far more controllable than other underwater inspection systems currently available.

The new system is code-named SMARTIE (Submarine Automatic Remote Television Inspection Equipment). It is elliptical in cross-section and is basically a highly mobile underwater vehicle equipped with a battery of underwater television cameras. These will consist of at least one low-light silicon intensified target (SIT) camera and a high resolution vidicon camera. The vehicle is driven by an electrically-powered submersible pump and is therefore propellerless.

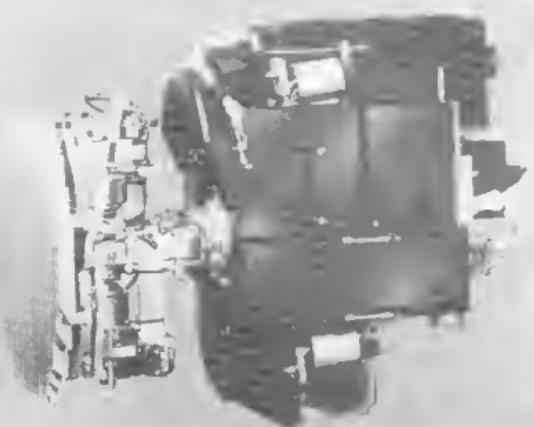
On-Board Computer

The addition of on-board computer facilities has enabled Marine Unit to provide the offshore industry with a submersible which is much more powerful and versatile than has been available to the industry in the past. The microcomputer was designed and developed by Marine Unit Technology's research and development team headed by Dr. Brian Ray. This is the first occasion on which a microcomputer has been installed on an underwater vehicle of this type.

Apart from the relatively straightforward procedures of interpreting manual input control signals from the operator's console, and controlling vehicle speed and direction, the computer is also capable of making SMARTIE a good deal easier to operate. For low visibility work, the computer can accept input from the submersible's magnetic compass and gyro, and project an artificial navigation 'target' which the operator can follow on his video screen even though the craft may be passing through an area of zero visibility. Similarly, if the submersible is operating in fast currents, the operator is able to maintain a fixed position in the water by simply pressing a 'hold' button: the computer will automatically compensate for the effects of the current, keeping the vehicle in the required position without operator intervention. The 'hold' facility is also useful for keeping a steady course at speed.

Slim Umbilical Cable

The vehicle will be supplied with power and control signals by a single umbilical cable under half a centimetre in diameter. The video signal will be continuously transmitted back to the surface via the same cable. Most unmanned submersibles are supplied by very bulky multi-core cables bearing separate conductors for the



elektor



control circuits, power circuits and video controls and signals. This configuration can affect the performance of the vehicle adversely in a number of different ways.

Firstly, there is a very real problem of physical drag exercised by the cable on the vehicle, secondly, there is the problem of interaction between the video, control and power circuits, a problem which can cause interference or other deterioration in video picture quality.

Careful design of the electronics has ensured that these problems do not occur, and at the same time has made it possible to keep the cable dimensions to a minimum.

Projected Developments

Marine Unit will eventually be offering a number of different services to the offshore industry, and the next phase is already under development. One facility will be to enable the vehicle to 'lock-on' and follow closely a pipeline or other submerged structure at a fixed distance from it. It is also hoped to fit sonar equipment at some later date.

Offshore Survey Service

SMARTIE will not be sold to the offshore industry for the time being. Instead, MUI's Associate Company Marine Unit Limited will offer a complete inspection service to the offshore industry. It is expected that the main applications will be in surveying pipelines, underwater construction work, and other work where the cost of putting a man on the sea-bed is becoming very expensive. SMARTIE will be made available in one of two operating modes. Firstly, it will be available anywhere in the world as an emergency model air transport kit, consisting of the SMARTIE submersible and electrical generator, operator's console and cable. Three trained SMARTIE operators will accompany the submersible. SMARTIE will also be

available for long-term contracts with a custom-built winch and a robust launcher which will be designed to withstand very rough surface conditions; in this mode, SMARTIE will be launched at depth and a prefabricated building will house all the controls. Marine Unit will have available two SMARTIE units by the end of July, with others following later in the year. All the production models will be manufactured at the Group's new Plymouth factory.

SMARTIE should provide the offshore operator with a very realistic low-cost alternative to the diver used as an underwater observer, even in shallow water. Over the years it has been proven that an operator on the surface actually sees more on his screen than the diver on the sea-bed. Now SMARTIE gives the Television camera the mobility, the precision and the manoeuvrability of the diver. In addition, SMARTIE can operate in more hazardous conditions than the diver.

*Marine Unit Technology Ltd
3 Friars Lane, Richmond
Surrey TN9 1NL, England*

(348 S)

puffometer

Obviously, the length of time one can continue to whistle a particular note depends on how loud one tries to whistle and on how much air from the lungs is available to sustain the note. These factors determine the basic principle of the puffometer, which provides a comparative indication of different people's lung capacity by measuring how long they can sustain a note above a particular level. A multimeter is used to provide an optical indication of the duration of the signal. It goes without saying that the puffometer is not intended to be a serious scientific instrument, but rather is suited for 'party-piece' applications (where the reader may well find that his performance on the puffometer is determined more by his ability to keep a straight 'pucker' than the capacity of his lungs!).

Block diagram

The block diagram of the puffometer is shown in figure 1. As can be seen, the circuit is comprised of a number of different stages, each of which will be examined separately.

The whistled note is picked up by a microphone, which of course, converts it into an electrical signal. This is then fed to the lowpass filter, block 1, which removes the high frequency interference components from the signal which could be generated by nearby electrical appliances.

Block 2 contains an amplifier with a gain of between 50 and 500. Once the signal has been amplified it is fed to a bandpass filter with a centre frequency of 1900 Hz. This means that signals with a frequency of 1900 Hz are passed unaffected, whilst frequencies above and below this figure are attenuated. The filter output signal is then rectified by the circuit in block 4. The waveform of the whistled note is basically a sinewave, i.e. it contains positive and negative half cycles. During the negative cycles when the diode is conducting, the capacitor, C6, rapidly discharges (under quiescent conditions the capacitor is held charged via R9).

The output of the rectifier is fed to a comparator, which, as its name suggests,

Spirometers, which are instruments designed to measure a person's lung capacity, are both fairly complicated and expensive devices, and would be difficult to construct at home. The 'puffometer' described in this article, whilst making no claims to providing accurate volume measurements, nonetheless represents a relatively simple (and amusing) means of comparing how much air different people can expel in a single breath by measuring how long they can hold a whistled note.

Figure 1. The block diagram of the puffometer. The numbering of the blocks is repeated in the circuit diagram of figure 2.

Figure 2. The complete circuit diagram of the puffometer. The input signal is picked up via a crystal microphone and a multimeter is used for the read-out.

Figure 3. The power supply for the puffometer. The power supply circuit is also used to derive the 5 V reference voltage. With the exception of the transformer, bridge rectifier and smoothing capacitor, the power supply is mounted on the p.c.b.

compares the capacitor voltage with a preset reference voltage, UR.

As soon as the capacitor voltage falls below the reference voltage, the output of the comparator swings low. This causes the LED to light up, thereby indicating that the amplitude of the whistled note is sufficiently large and of the correct tone to be processed by the puffometer. As long as the comparator output is low, the capacitor in block 6 remains discharged; the start button is pressed, the output voltage of the integrator starts to rise. This voltage is then displayed on a meter.

When the input signal to the microphone stops, the capacitor in block 4 once more charges up, taking the output of the comparator high, extinguishing the LED and causing the capacitor in block 6 to also charge up. The time taken for this capacitor to charge fully is determined by the value of the capacitor itself and of the series resistor, block 6 is therefore basically a delay network. When the capacitor voltage reaches a certain value, the output voltage of the integrator ceases to rise and is held at whatever level it has reached at that moment. This means that the meter reading will be held until it is reset.

When a second person wishes to test his 'puff power', the pushbutton is depressed, resetting the meter.

Circuit diagram

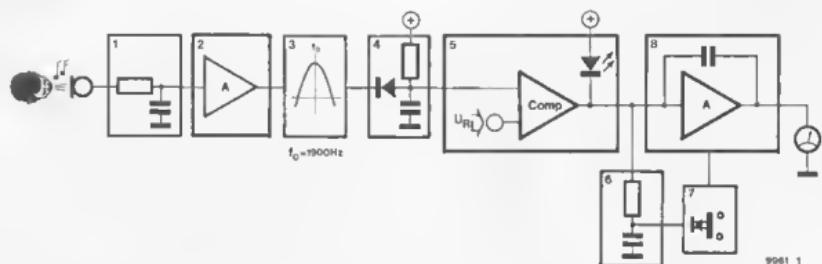
The complete circuit diagram of the puffometer is shown in figure 2. The microphone signal is fed via the DC decoupling capacitor, C1, to the lowpass filter formed by R2 and C2. Signals with a rise time shorter than 470 ns, i.e. frequencies greater than 340 kHz, are suppressed.

A1 is the amplifier of block 2. The gain (A) of the amplifiers equals

$$A = \frac{R_4 + P_1}{R_3} + 1,$$

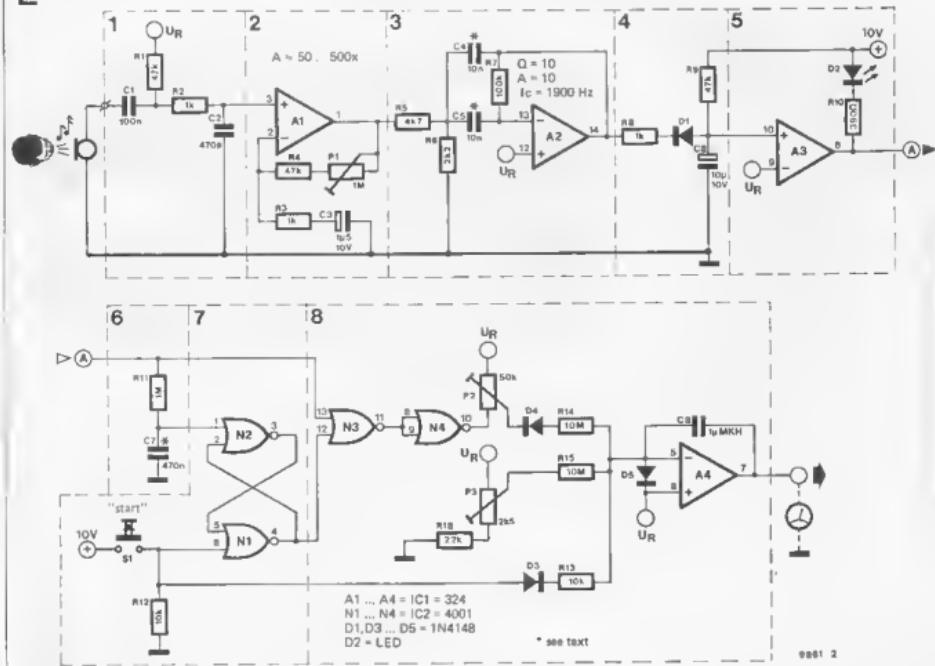
which means that P1 can be used to vary the sensitivity of the puffometer. The output voltage of the amplifier is divided across R5 and R6, and fed via C5 to the bandpass filter circuit round A2. The negative feedback loop (i.e. a

1



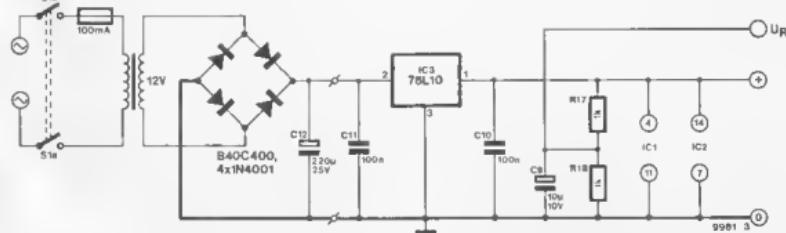
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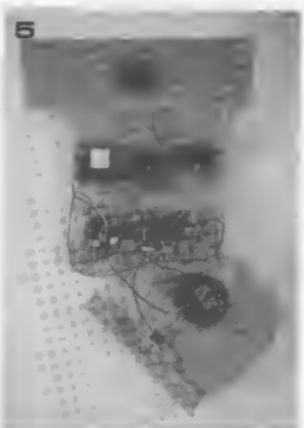
9981 3

Figure 4. Track pattern and component layout of the p.c.b. for the puffometer (EPS 9661).

Figure 5. The interior of a finished model of the puffometer. Care should be taken to ensure that the 240 V connections are safely insulated.

Figure 6. An inexpensive alternative to a multimeter can be formed by using a 100 μ Ameter and a current-limiting resistor. Full-scale deflection should be obtained at an output voltage of roughly 7 V. If a 1 mA instrument is used, the value of the current limiting resistor should be 6 k Ω .

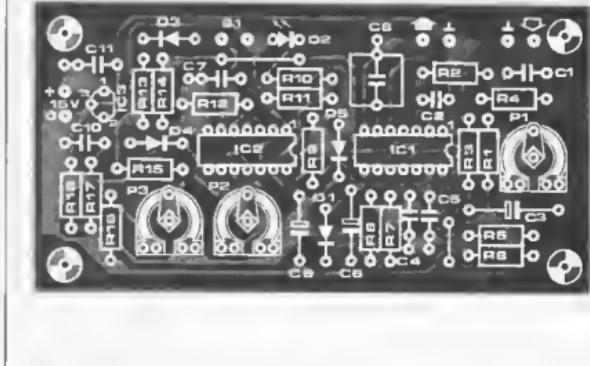
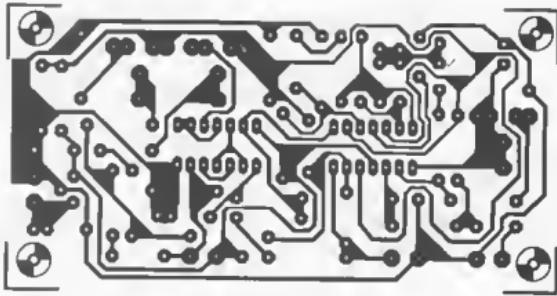
Figure 7. A modern and attractive case for the puffometer can be constructed using perspex and a little skill.



portion of the output signal is fed in antiphase back to the input) via C4 and R7 ensures that, just as the gain of A1 could be varied by altering the value of the feedback components, so the gain of A2 varies with the frequency of the input signal. The values of the various components were chosen so that at approx. 1900 Hz A2 would have maximum gain.

The output of the filter is fed to the peak rectifier circuit of block 4. Under quiescent conditions C6 is kept charged via R9. When the microphone picks up an input signal, C6 will be discharged via D1 whenever the output of the 1900 Hz filter goes low (i.e. negative). Since R8 is much smaller than R9, the capacitor discharges much more rapidly than it charges, so the voltage on C6 is lower than that of the reference voltage. The comparator, A3, has no feedback, which means that it has a very high gain. The difference between the reference voltage on the inverting input and the voltage across C6, on the non-inverting input, is amplified to such an extent that it is either 'high' or 'low'. When it is low current flows through R10 and the LED, D2, which causes it to light up.

4



If the voltage across C6 exceeds the reference voltage of the comparator, however, the output of the comparator will swing up to plus supply. The result is that there is no longer a voltage drop across R10 and D2, hence the LED goes out. This indicates that either the whistler has stopped whistling or is whistling at the wrong frequency.

The circuit round N1, N2 and the pushbutton S1 forms a flip-flop. The voltage level at pin 4 is determined by the voltage levels at pins 1 and 6. Under quiescent conditions, the output of A3 is high, so that capacitor C7 is charged up via R11. Pin 1 of N2 is therefore high, whilst pin 6 of N1 is low (S1 is normally open), with the result that the output of N1 (pin 4) is also high.

As soon as the microphone picks up an input signal, the voltage on C7 falls; if the start button is then pressed, pin 6 of N1 is taken high, with the result that the output of N1 goes low, as does pin 2 of N2. This means that, as long as an input signal is present and C7 is discharged, the output of N2 is held high, so that even after the pushbutton has been released, the output of N1 remains low.

N3 monitors the output states of the

flip-flop and of the comparator, A3. Initially these are both high, so that the output of N3 is low, with the result that the output of inverter N4, is high. Although a current flows through P2, D4 is reverse biased and ensures that no current flows to A4. When an input signal is present, the outputs of A3 and of the flip-flop are low, so that the output of N3 is high, and that of N4 is low.

With no input signal the voltage at both inputs of A4 is virtually the same (U_R). The input bias current setting of the op-amp is such that a small current flows from the inverting input via R15, P3 and R16 to earth. This current is just sufficient to keep C8 charged.

When the output of N4 goes low, i.e. falls below U_R , current attempts to flow from the inverting input of A4 through R14, D4 etc. Due to the high input resistance of the op-amp, however, this current can only be supplied round the negative feedback loop. The output voltage of the op-amp therefore swings positive to hold the voltage at both inputs the same. C8 first discharges then charges up with reverse polarity. The time taken for the output of the op-amp to swing high is determined by

parts list to figures 2 and 3

Resistors:

R1, R4, R9 = 47 k
 R2, R3, R8, R17, R18 = 1 k
 R5 = 4k7
 R6 = 2k2
 R7 = 100 k
 R10 = 390 Ω
 R11 = 1 M (100 k)*
 R12, R13 = 10 k
 R14, R15 = 10 M
 R16 = 22 k
 P1 = 1 M preset potentiometer
 P2 = 50 k preset potentiometer
 P3 = 2k5 preset potentiometer

Capacitors:

C1, C10, C11 = 100 n
 C2 = 470 p
 C3 = 1 μ 5/10 V
 C4, C5 = 10 n
 C6, C9 = 10 μ /10 V
 C7 = 470 n (10 n)*
 C8 = 1 μ polycarbonate or
 polyester

Semiconductors:

A1 ... A4 = IC1 = 324
 N1 ... N4 = IC2 = 4001
 IC3 = 78L10
 D1, D3 ... D5 = 1N4148
 D2 = LED

Miscellaneous:

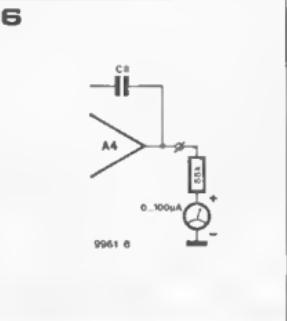
transformer 12 V, 500 mA secondary
 bridge rectifier 40 V/400 mA or
 4 x 1N4001
 electrolytic capacitor 220 μ /25 V
 S1 = pushbutton, push-to-make
 F1 = fuse 100 mA
 double-pole on/off switch
 microphone
 if used: 100 μ A-meter
 68 k* resistor

* see text

the time constant C8/R14. The rise in the output voltage of A4 can be measured on a multimeter. As soon as the input signal ceases, the output of N4 is once more taken high, D4 is reverse biased, and thanks to the small bias current from the inverting input of A4, the voltage on C8 is held at that instantaneous value (provided P3 is set correctly). The meter reading can then be checked at leisure. Pressing the start button has the effect of returning the inverting input of A4 to U_R , so that the output falls back to zero, thereby restoring the original polarity of C8. The reference voltage U_R is derived from the supply, the circuit diagram of which is shown in figure 3. As can be seen, a 10 V IC regulator is used. R17 and R18 divide down the regulated 10 V supply to derive a 5 V reference voltage.

Construction

The track pattern and component layout of the p.c.b. for the puffometer are shown in figure 4. The component numbering in this figure corresponds to the numbering in figures 2 and 3. The transformer, four rectifier diodes (or a



single bridge rectifier) and the 220 μ F electrolytic are not mounted on the board. The photograph shown in figure 5 indicates how these can be mounted safely and compactly beside the p.c.b.

The ICs are best mounted using sockets; this reduces the risk of overheating the IC pins during soldering.

The centre frequency of the bandpass filter, and hence the desired pitch of the required whistled note, can be varied by altering the values of C4 and C5. A smaller value will increase the centre frequency whilst a larger value will decrease it.

There is a certain delay between the moment a person stops whistling and the needle on the meter settling at a final reading. This delay is determined by the time taken for C7 to charge up. It is therefore possible to increase the duration of this interval by increasing the value of C7. It is even possible for the skilled owner of the puffometer to cheat a little by selecting a value for C7 which allows him to take in a quick breath in the middle of his attempt!

If the above mentioned cheat function isn't desired the unit's operation can be

changed by substituting a 10 n capacitor for R11 and by replacing C7 with a 100 k resistor. If this change is incorporated then the function of S1 is changed. By pressing S1 once the meter is reset to zero. Once the whistling starts and the LED lights the meter should start to climb, but once the whistling stops, however briefly, the meter reading is frozen, thus thwarting any cheaters.

Any normal type of microphone, such as those used with cheap cassette recorders will prove suitable.

A multimeter set to the 10 Volt DC range can be used as the readout indicator for the puffometer. Or, if available, the LED voltmeter described in Elektor 12, April 1976 could also be used, or a panel meter with suitable range resistors like that shown in figure 6 will also work nicely.

Calibration

Calibrating the puffometer is a relatively simple matter, since there are only three potentiometers which require adjustment.

To start, P1 and P2 should be turned fully anticlockwise. LED, D2, should now be lit. Now, whistle very softly into the microphone, the meter should rise fairly fast, when a reading of about 5 Volts is reached, stop whistling. The meter reading should be stable, i.e. not falling or rising. If the reading is not stable adjust P3 one way or the other so that the reading is frozen, not drifting. Now, P1 and P2 can be adjusted. P1 adjusts how sensitive the microphone is, and P2 controls the rate or speed the meter climbs to full scale. P2 should therefore be adjusted such that the needle is deflected slowly enough that the most long winded person just runs out of breath before the meter reaches maximum reading. P1 is adjusted so the unit isn't too sensitive, otherwise it might respond to background noise.

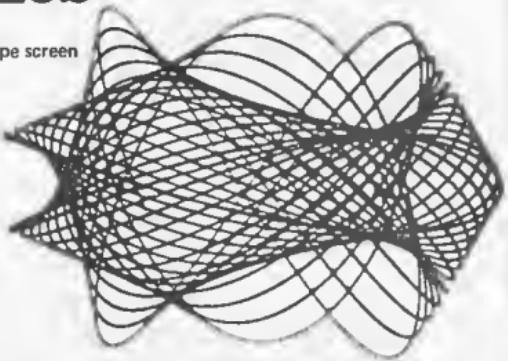
Operation

If the unit is wired as shown in the circuit of figure 2 then S1 functions as follows. S1 should be pressed and held until the whistling starts and the LED lights, then it should be released.

If the unit is modified (R11 and C7 changed) then S1 should be pressed to reset the unit and then released. Once the whistling starts and the LED lights, the meter will start automatically.

oscillographics

Fascinating geometrical patterns on an oscilloscope screen



The accompanying illustrations give some idea of the variety of different patterns that can be generated by the 'spirator' (spirographics generator). As can be seen, they are similar to the patterns which can be produced by hand using the popular 'Spirograph™' outfit, and also to the type of figures often produced by computer graphics. The patterns are derived from certain basic geometrical functions, and are known as 'Lissajous' figures. They are to be found in nature, for example in the path described by an object fixed to the end of a rope which is oscillating. In geometrical terms a Lissajous figure is obtained when a point describes a sinewave on both the X- and Y-axes. The circuit of the spirator produces two sinewave voltages, the frequency of each being independently variable. Both sinewaves are damped, i.e. after the waveform has been started, the function will decay exponentially to zero.

Block diagram

The function of the spirator can be explained simply by referring to the block diagram of figure 1.

The circuit is built round two damped-sinewave oscillators, one of which is responsible for the vertical deflection (Y-signal) of the spot on the screen, the other for the horizontal deflection (X-signal). Both the frequency and the degree of damping of the two oscillators are independently variable by means of potentiometers. It is also possible to modulate either oscillator frequency by an external signal, so that the patterns are continuously changing.

Since the oscillators are not free-running but have to be started, there is an astable multivibrator which ensures that both oscillators are triggered simultaneously. The trigger frequency is 60 Hz. Whilst the oscillators are being

An oscilloscope can be used not only as a test instrument; with the aid of the following circuit it can be made to generate a multitude of fascinating and attractive geometrical patterns.

M. Zirpel

started the spot on the screen is blanked by means of the brightness signal Z, thereby suppressing unwanted lines produced by the normal scan of the scope.

Circuit diagram

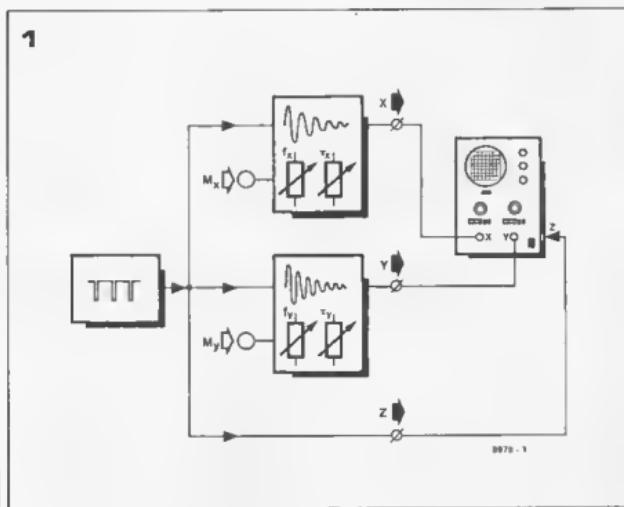
The complete circuit diagram of the spirator is shown in figure 2.

The astable multivibrator which provides the trigger pulses for the two damped-sinewave oscillators is formed by the simple circuit round opamp IC1. As was already mentioned, the frequency of the multivibrator signal is 60 Hz, sufficiently high to ensure a flicker-free picture on the scope screen. The period for which the output of IC1 is high is much longer than the period for which it is low. During the latter portion of the signal the trace is blanked via the brightness input. The next positive-going edge at the output of IC1 triggers the sinewave oscillators. The two oscillators are identical and consist of three 741 opamps. IC2, IC3 and IC4 comprise the oscillator for the horizontal (X-signal), whilst IC5, IC6 and IC7 form the vertical (Y-signal) oscillator. To see how they work let us take the example of the X-oscillator.

Opamps IC2 and IC3 are both connected as integrator and thus, at a certain frequency, produce a phase-shift of 180° in sinewave signals. A further phase-shift of 180° is introduced by IC4, which functions as an inverter. The three opamps together therefore have the total phase-shift of 360° required for oscillation. The total gain of the 3 cascaded opamps can be varied by means of P1 and is always less than unity. Thus, once started, the oscillator generates a damped sinewave. The degree of damping can be varied by means of P1 (P3 in the case of the Y-signal), and the frequency of the

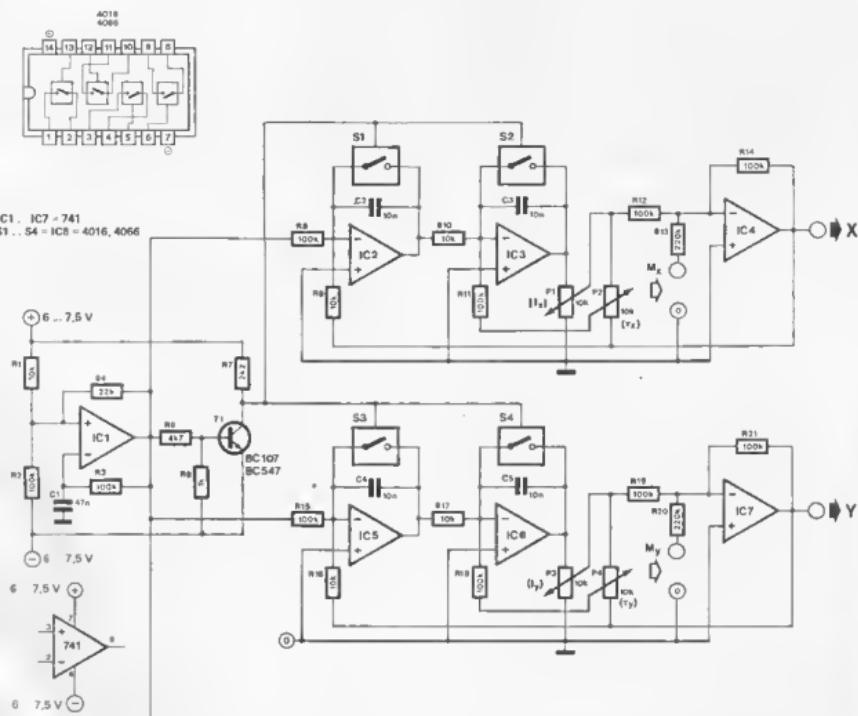
Figura 1. The spirographics generator consists of two damped-sinewave oscillators which are triggered by an astable multivibrator. Both the frequency and damping of the sinewaves can be varied independently. The oscillator output signals are used to control the X- and Y-deflection of an oscilloscope trace; the result is a fascinating display of Lissajous figures.

Figure 2. The complete circuit diagram of the spirograph. Two extra modulation inputs allow the pattern to be continuously varied. Various different types of oscillator (sinewave- or triangle-) can be used to provide the modulation inputs. Waveforms with steep edges (sawtooth, squarewave etc.) result in an abrupt transition from one pattern to another.



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9978-2

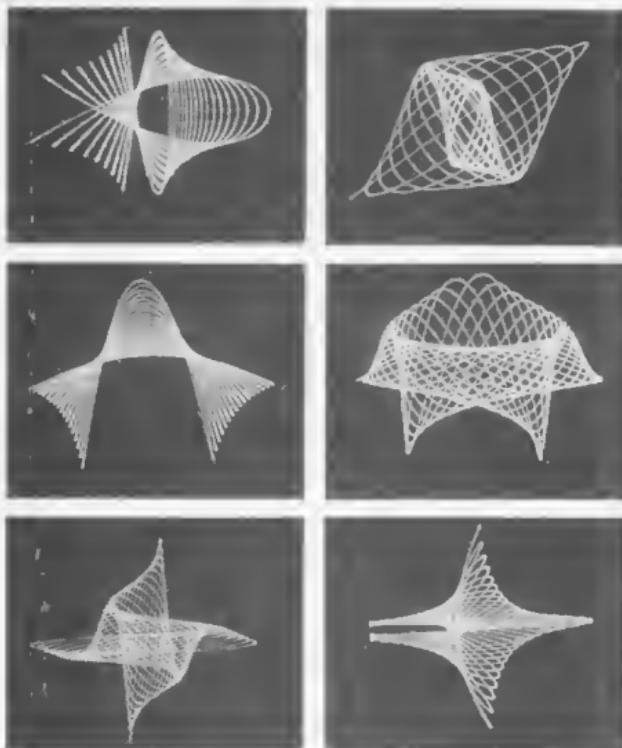


Figure 3. These photographs give some idea of the type of patterns which can be obtained from the spirograph.

oscillator can be adjusted by means of P_2 . In order to obtain a stable picture on the screen, both oscillators must, of course, be triggered simultaneously. This is ensured by means of electronic switches $S1 \dots S4$. At each positive-going edge of the output signal of $IC1$ they cause the capacitors $C2 \dots C5$ in the feedback loops of the opamps to be discharged. This sets the initial conditions of each opamp, i.e. that the output always starts from the same voltage. Thus each successive pattern written on the screen appears at exactly the same point thereby producing a completely stable image. Without this precaution, integrator drift would cause the same pattern to appear at slightly different positions on the screen — a highly undesirable effect.

The circuit also offers the particularly

aesthetic possibility of displaying moving patterns by varying the frequency and/or damping of one or both oscillators. To this end the circuit provides extra control inputs (M_1 and M_2) for low frequency modulation signals (from, e.g. a sinewave generator). Naturally enough, various types of signal (squarewave, triangle etc.) of varying amplitude and frequency can be used. The type of waveform will determine the design of the resulting pattern, the frequency will determine the speed at which it changes, whilst the amplitude affects the extent to which the pattern varies. The only constraint upon the modulation signal is that it should not contain a DC component (i.e. it should be symmetrical and AC coupled), otherwise there is the possibility that part of the pattern will be off the screen. The maximum amplitude of the modulation signal is 15 Vpp. If desired the value of $R14$ and $R21$ can be altered to suit input levels greater than this.

Depending upon the type of oscilloscope used, it may be necessary to invert the Z -signal, in which case the signal can be taken from the collector of $T1$. If the picture is not completely flicker-free, then the value of $C1$ should be reduced accordingly. ■

one chip does not make a piano

The General Instruments 'piano-IC' (the AY-1-1320) took some taming... Initially, several manufacturers of electronic musical instruments were interested in this chip. In particular, the ingenious keying system is noteworthy: the loudness of a note depends on the force with which the key is struck, as in a 'real' piano.

It was a great disappointment to discover that the designers were apparently satisfied with a signal-to-noise ratio that is more suited to digital circuits than to music. To give an idea, the permissible S/N ratios for a few technologies are as follows:

CMOS:	10 dB (30% logic level tolerance)
TTL:	10 dB (10% logic level tolerance)
stereo:	26 dB (5% crosstalk between channels)

'DIN HiFi': 50 dB (0.3%, S/N ratio) For electronic organs and the like, the unwanted signals (i.e. the output from all keys except the ones actually depressed) should be at least 50 dB down. To our great surprise, a prototype piano built according to the GI application note proved to have a S/N ratio closer to 10 dB! On contacting several electronic organ manufacturers, we discovered that they had encountered the same problem and — as far as our information goes at present — they have now all given it up as a bad job. However, our designers suffer from a stubborn streak. It took some doing, but they finally came up with a satisfactory circuit. Feedthrough of unwanted signals is reduced to the point where it is no longer audible (S/N better than 50 dB) by means of an additional electronic switch for each key. This does increase the price by about £3 for each octave, which is a pity. Perhaps GI could consider designing an improved version of the original chip, or possibly a second add-on chip for the gating? Anyway, we've finally found a circuit that works — and that's quite a relief. ■

master tone generator

Keyboard instruments use the equally tempered scale, in which each octave is divided into twelve semitones. Any two adjacent semitones differ in frequency by a ratio $\sqrt[12]{2}:1$, or 1.0594631. Notes 12 semitones or one octave apart obviously differ in frequency by a factor $(\sqrt[12]{2})^{12}$, i.e. 2. Since it is not really practical to use a separate oscillator for each note of a keyboard instrument, it has been common practice for a number of years to use separate oscillators to generate the twelve notes of the top octave, and then by the process of frequency division, by powers of two, the lower octaves can be derived.

More recently it has become possible to replace the twelve top octave oscillators by a single master oscillator which generates the twelve top notes from a single (crystal-controlled) clock. The advantages of this approach are obvious. Firstly, since the top octave notes are locked to the clock generator and the lower octaves are locked to the top octave, a single adjustment serves to tune the whole instrument. This greatly simplifies the setting up procedure and allows the instrument to be tuned easily to other instruments. Secondly, the use of a crystal clock allows excellent stability of tuning.

The master oscillator is necessarily more complex than the octave dividers which follow it. It is not possible to generate, say, top C and then divide by 1.0594631 to obtain B, since digital frequency dividers can divide only by integral numbers. The solution is to derive both C and B (and all the other notes) by dividing down from a much higher clock frequency. For example, dividing 1 MHz by 239 gives 4184.1 Hz or c^8 , whilst dividing by 253 gives 3952.6 Hz or b^5 , and so on. The frequency ratio between these two notes is 1.05858, which is a reasonable approximation to a semitone. A more accurate approximation could, of course, be obtained by using longer divisors, but this would, of course, entail raising the clock frequency and using longer divider chains.

For a more detailed discussion of these points readers are referred to the article 'Digital Master Oscillator' in Elektor 9 and 10, January and February 1976.

It is possible to design a master oscillator

Although primarily intended for use in the Elektor piano described elsewhere in this issue, the design of this master tone generator is sufficiently universal to permit its use in a wide variety of electronic keyboard instruments.



using standard logic circuits, but fortunately ready-made master oscillators exist in the form of the General Instruments AY-1-0212 IC and the equivalent Motorola M 087 IC. These ICs operate on the principles described above.

The complete circuit of the master tone generator is given in figure 1. A 1 MHz crystal oscillator based on inverters N13 and N14 provides the master clock frequency. The output of N14 is squared up by a Schmitt trigger built around N15 and N16, the output of which drives the clock input of the master oscillator, IC13. The clock frequency is divided down by the ratios shown to give the twelve notes of the top octave, the twelve outputs being buffered by inverters N1 to N12.

The twelve buffered outputs are fed to the top octave output connections of the master tone generator, and also to twelve, seven-stage CMOS binary counters which provide the outputs for seven lower octaves, giving the master tone generator a compass of eight octaves, from $C_2 = 17.3$ Hz to $c^5 = 4148.1$ Hz, which should be adequate for even the most ambitious instrument. No vibrato is provided on the master oscillator since the output of the master tone generator may be used for both the manuals and pedals of an organ. If vibrato is added to the low pedal notes of an organ the effect is most unpleasant. A much better idea is to add vibrato and/or tremolo to the manual outputs using a Leslie speaker or an electronic vibrato system such as the 'Phasing and Vibrato' unit featured in Elektor 20, December 1976.

Construction

Although the design of the master tone generator may be unremarkable, the construction is worthy of note, since the entire circuit is mounted on a single p.c. board only 12.5 cm x 16 cm. This small size is achieved by the use of a double-sided p.c.b., the layout of which is shown in figure 2. To keep costs down plated-through holes are not employed, and all through connections are made using wire links. The pads where such a through connection is to be made are identified on the com-

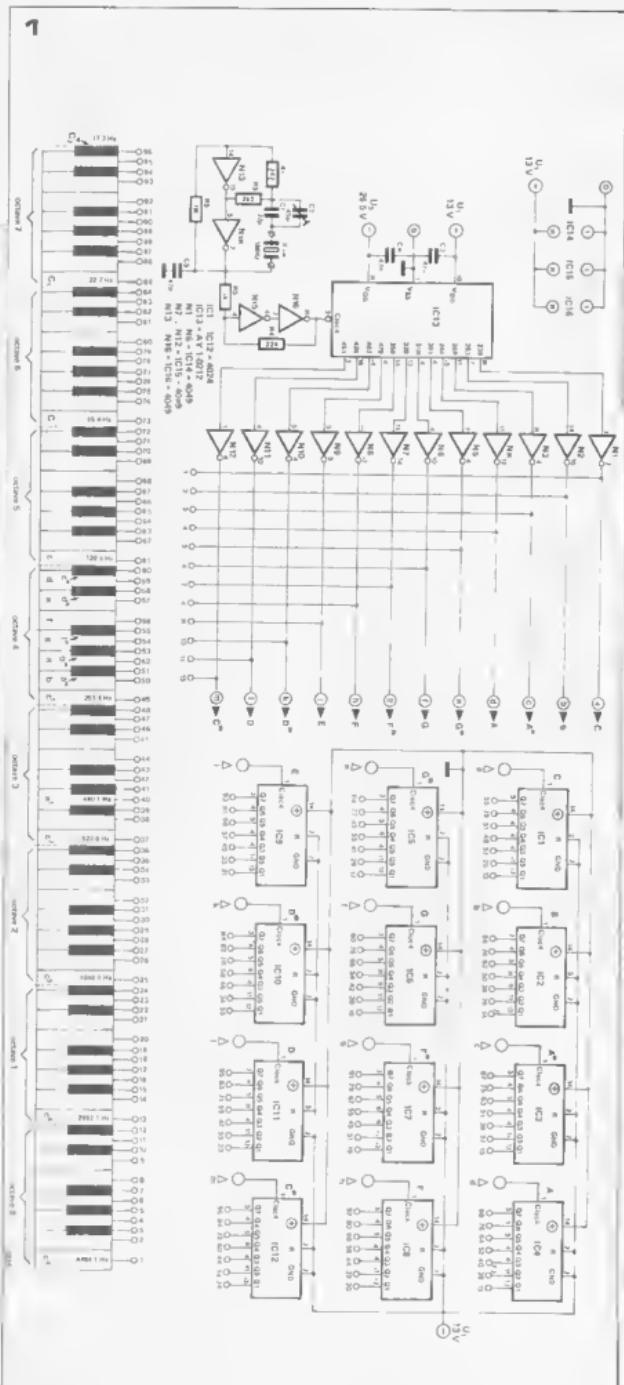


Figure 1. Complete circuit of the master tone generator.

Figure 2. The complete tone generator circuit is mounted on a single p.c. board only 16 x 12.5 cm (EPS 9915).

Parts list

Resistors:

$$\begin{aligned} R1, R2 &= 2k\Omega \\ R3 &= 1\text{ k}\Omega \\ R4 &= 22\text{ k}\Omega \\ R5 &= 1\text{ M}\Omega \end{aligned}$$

Capacitors:

C1 = 27 p
C2 = trimmer 45 p
C3,C4 = 47 n
C5 = 47 p

Semiconductors.

IC1 . . . IC12 = CD 4024
IC13 = AY-1-0212 or M 087
IC14 . . . IC16 = CD 4049

Miscellaneous

1 MHz crystal \approx 30 pF

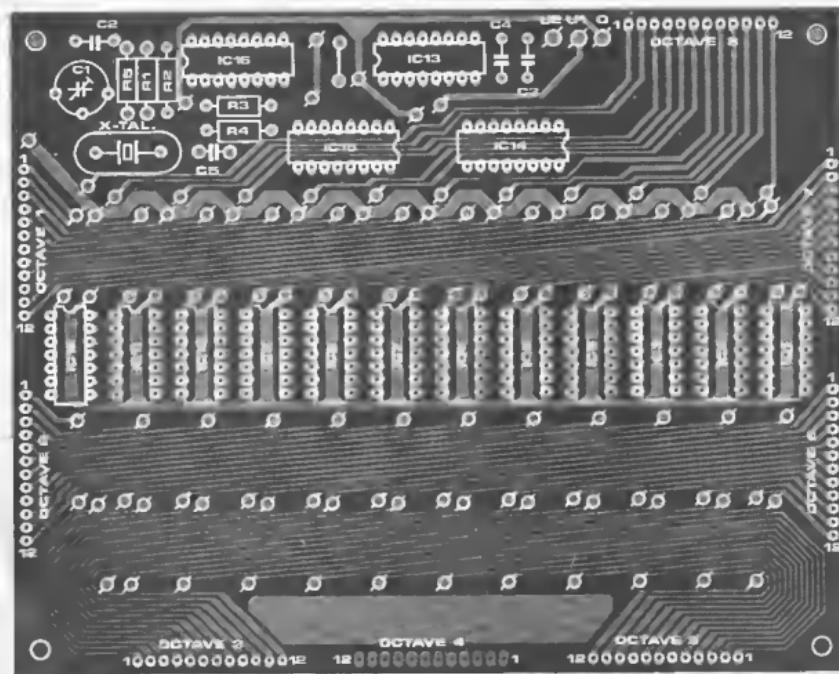
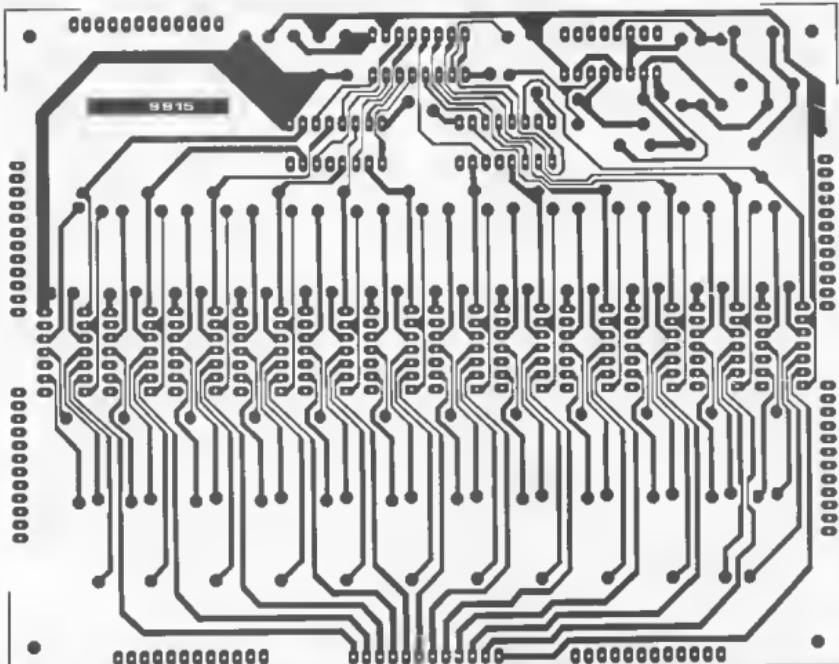
ponent layout by the symbol \emptyset . The other components are soldered on the reverse side of the board only, i.e. no solder joints are made on the component side of the board except to the wire links.

An interesting feature of the board is that the 12 outputs for each octave are brought out in the correct order so that they can be connected direct to the piano using 12-way ribbon cable. Since the ICs used in the master tone generator are MOS or CMOS devices special handling precautions should be observed when constructing the unit.

Tuning

The only tuning adjustment is to vary trimmer C2 until the oscillator frequency is exactly 1 MHz, when the tone generator will be tuned to international concert pitch ($a^1 = 440$ Hz). This can be done by connecting a frequency counter to the output of N16. Alternatively, if a frequency counter is not available then a^1 can be adjusted to 440 Hz using a tuning fork. This exact tuning procedure is not absolutely necessary for normal domestic use. Since the outputs of the tone generator are locked to the clock oscillator the relative tuning is always correct, i.e. the tone generator is in tune with itself, even though the overall absolute tuning may be slightly sharp or flat.

2





electronic piano

The principal difficulty in simulating the unique sound of a piano is caused by the touch sensitivity of the keys. When a key of an organ is depressed the loudness of the note produced is fixed, irrespective of how hard the key is struck, and the note continues with the same volume until the key is released, whereupon the note dies away more or less rapidly.

The key action of a piano, on the other hand, is much more complex. The strings of a piano are struck by felt-covered wooden hammers actuated by the keys. The number of strings associated with each note varies over the compass of the keyboard. For example, at the bass end each hammer strikes only a single string, whilst there may be as many as three strings per hammer in the middle and treble registers. The strings for each note are equipped with a felt damper, which is raised when a key is pressed and falls back when the key is released. The loudness of a note played on a piano is determined by the final velocity of the hammer as it strikes the strings, which is determined by how hard the key is struck. This also affects the harmonic content of the note, but this is difficult to simulate electronically and only touch sensitive loudness is normally provided on electronic pianos. When a key is struck on a piano the sequence of events is as follows: the damper is lifted from the strings and the hammer strikes the strings with a velocity dependent on how hard the key was struck, then falls back. The note sounds with a rapid, percussive attack and then decays gradually over a period of several seconds, unless the key is released, in which case the damper falls back and the note is terminated rapidly. A piano is also equipped with two pedals. The sustain pedal holds the dampers off all the strings, even when the key is released, and thus prevents rapid termination of a note with key release. The soft pedal reduces the loudness of the notes, either by shifting the whole keyboard sideways in the case of a grand piano, so that the hammers strike less strings, or by reducing the hammer travel in the case of an upright piano. The envelope which the output of a piano follows is shown in figure 1. The amplitude dynamics of a piano can be simulated electronically, though the

Although electronic organs have existed for many years, it is only with the advent of semiconductors, and in particular, integrated circuits, that an electronic simulation of a piano has become possible. Over the past few years electronic pianos have rapidly grown in popularity, thanks largely to their compact size and relatively low cost compared to a conventional instrument. The Elektor piano offers all the facilities of a conventional piano, i.e. touch sensitive keying and pedals, plus a choice of three different voices, normal piano, honky-tonk piano and harpsichord. A modular design allows the constructor to build a piano with as many octaves as required.

circuits to achieve this are considerably more complicated than the equivalent keying circuits of an electronic organ. However, the dynamic harmonic structure of the piano sound is a different proposition. As mentioned earlier the initial harmonic content of a note depends on the hammer velocity, and the harmonic content also changes as the note decays. In addition, due to the multiple stringing, a note may be produced by up to three different strings, which do not vibrate exactly in unison and so give rise to a complex pattern of beat notes.

Sympathetic resonances may also occur between the strings for different notes, especially if the dampers are lifted by using the sustain pedal, and resonances of the frame and case of the piano also contribute to the tonal quality. It is therefore obviously not a feasible proposition to attempt a complete simulation of the harmonic character of a piano, as this would be not only very difficult but also rather expensive.

Fortunately, it is possible to obtain a fairly good approximation to a piano sound by using relatively simple tone-forming circuits, and although the electronic piano is unlikely to replace the conventional instrument in the (classical) concert hall, it nonetheless has a number of advantages in other situations.

As mentioned earlier its cost is considerably less than that of a conventional piano, between a quarter and half the price of an upright type. The compact size and portability of an electronic piano will appeal to itinerant musicians and to those with limited dwelling space, and finally, by using headphones it is possible to practice on an electronic piano without disturbing one's family or neighbours.

Block diagram

A block diagram of the Elektor piano is shown in figure 2. As can be seen from this diagram the compass of the instrument is 5 octaves, as opposed to 7½ octaves for a conventional upright piano or 6½ octaves for some compact, modern, upright instruments. The frequency range of the Elektor piano is from C# = 69 Hz to c⁴ = 2092 Hz, i.e. the middle 5 octaves of a conventional piano. This somewhat restricted compass

does not greatly detract from the versatility of the piano, since the top and bottom octaves of a piano are used only infrequently, and it was felt that 5 octaves represented a reasonable compromise between performance, size and cost. Furthermore, 5 octave keyboards are readily obtainable, whereas 6- or 7 octave keyboards are not. However, since the construction of the piano is modular it is a relatively simple matter to tailor the compass as required.

The basic signals used in the Elektor piano are squarewaves. These are obtained at the correct frequencies from a digital master oscillator, which generates

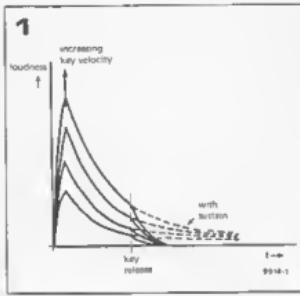
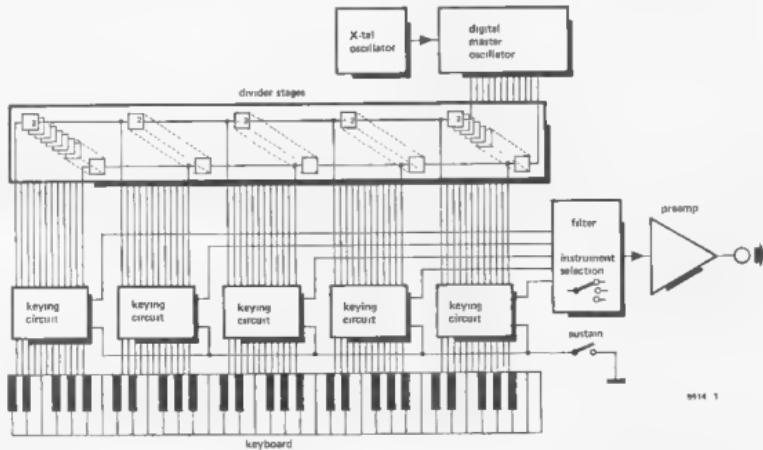


Figure 1. Envelope of a piano, showing how initial loudness increases with key velocity, and the effect of the sustain pedal.

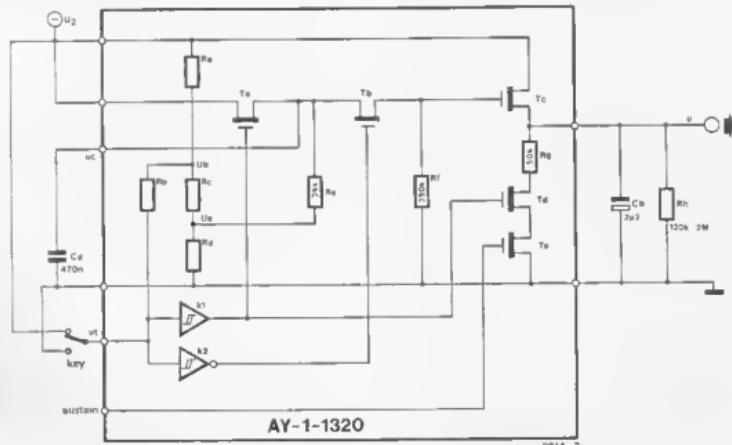
Figure 2. Block diagram of the Elektor piano.

Figure 3. Circuit of one envelope shaper stage, showing the internal arrangement of the AY-1-1320.

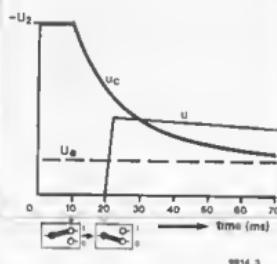
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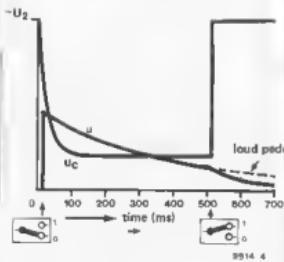
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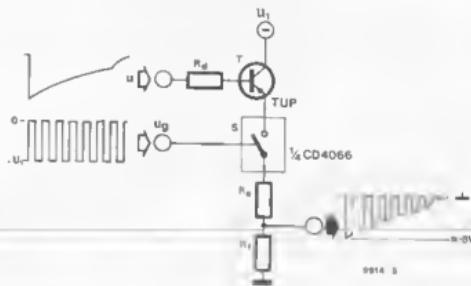
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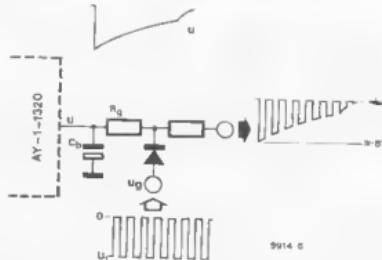
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7



the 12 notes of the top octave, and 12 multi-stage frequency dividers, each of which divides one output of the master oscillator by 2, 4, 8, 16 etc. to obtain the lower octaves. This master tone generator system is equally suitable, not only for the Elektor piano, but also for an organ or other keyboard instrument, and has therefore been made the subject of another (separate) article in this issue, see 'Master tone generator'.

Each output of the master tone generator is fed to a touch-sensitive keying circuit, one for each note of the piano. Each of these consists of a chopper circuit and an envelope shaper whose output follows the attack-decay-release contour of a piano. The envelope shaper output is fed to the chopper circuit which is driven by the appropriate output of the master tone generator. The resulting output of the chopper circuit is thus a squarewave whose amplitude follows the output of the envelope shaper.

The touch-sensitive envelope shapers are based on the General Instruments AY-1-1320 IC. Each of these ICs will provide touch-dependent keying for 12 notes, so one keying-circuit board containing an AY-1-1320 is required for each octave of the piano.

The outputs of the keying circuits for each octave are summed and fed to filters and voicing circuits which tailor

the harmonics of the output waveform to provide piano, honky-tonk or harpsichord sound. Finally, the filter outputs are fed to a buffer preamplifier which allows the piano to be interfaced to a suitable power amplifier.

Envelope shapers

Figure 3 shows the circuit of one envelope shaper. The section of the circuit enclosed by the bold line is contained within the AY-1-1320 IC and each IC contains 12 such circuits, so it is easy to see why these ICs have revolutionised electronic piano design.

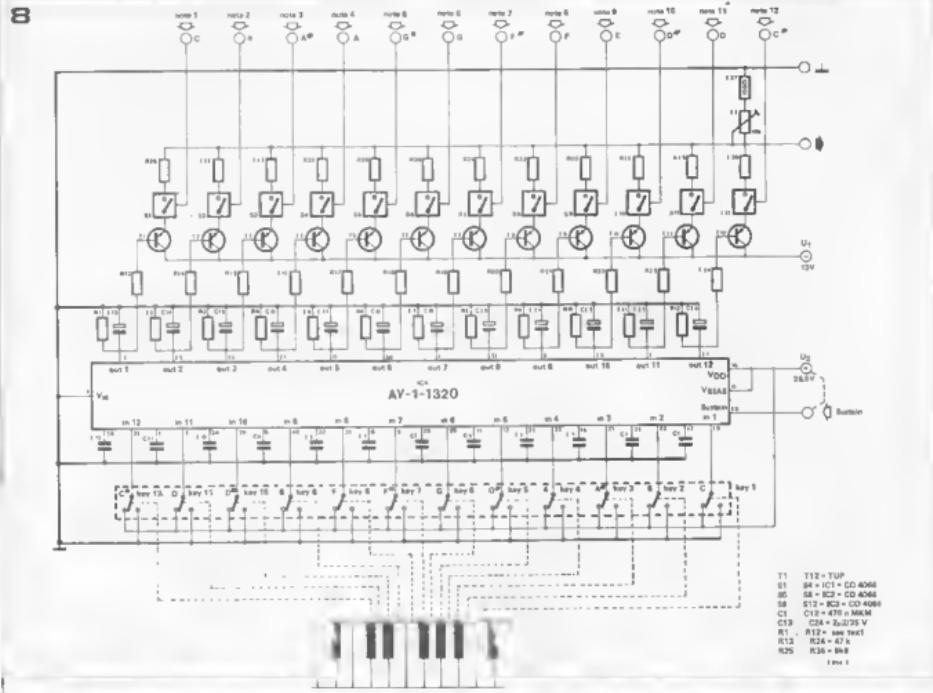
Each piano key is equipped with a set of break-before-make changeover contacts, and the circuit senses key velocity by measuring the time taken for the moving contact to change over from its rest position (normally closed) to connect with the normally open contact. The initial output voltage of the envelope shaper (before it begins to decay), is inversely related to the key travel time and is therefore directly related to key velocity.

Operation of the envelope shaper is as follows: firstly, it should be noted that the AY-1-1320 is a MOS IC and operates from a negative supply voltage. The position of the key contact is sensed by two comparators, k_1 and k_2 . When it is in the rest position the moving contact is connected to U_2 , the negative supply voltage. This voltage is below the

thresholds of both comparators, so the output of k_1 is low (negative), whilst the output of k_2 , which is an inverting comparator, is high (zero volts). T_a and T_d are turned on, whilst T_b is turned off. Assuming that T_e is turned on via the sustain input, the result is that the output capacitor, C_b , is held in a discharged state via R_g , T_d and T_e (output voltage U is zero) whilst timing capacitor C_a is charged to U_2 via T_a . When the key contact begins to move the moving contact breaks its connection with U_2 and the input voltage to the comparators now rises to U_b , which is set by R_a , R_c and R_d . This voltage is above the threshold of k_1 but below the threshold of k_2 , so the output of k_1 goes high whilst that of k_2 remains so. T_d turns off and T_a also turns off, with the result that C_b is no longer supplied via T_a and begins to discharge rapidly via R_e to U_a , the voltage set at the junction of R_c and R_d .

When the moving contact closes, the comparator inputs are connected to zero volts and the output of k_2 goes low, turning on T_b . The voltage on C_b is thus applied via T_b to the gate of source-follower T_c . This voltage, slightly attenuated due to the less than unity gain of the source-follower, appears at the source of T_c and causes C_b to charge rapidly.

The voltage remaining on C_b by the time the key contact closes, and hence



the voltage transferred to C_b , is logarithmically related to the key velocity. The higher the key velocity the faster the key contact will change over and the less C_a will have discharged, so the greater will be the voltage transferred to C_b .

This is illustrated in figure 4, which shows C_a discharging over about 60 ms when the key is operated, and the output voltage U rising as C_b charges when the key contact closes.

After the initial pulse, C_b receives no further charge from T_c , since the voltage U_c decays very rapidly and T_c turns off. C_b now begins to discharge through resistor R_h over a period of several hundred milliseconds. The value of R_h is varied over the compass of the keyboard, being smallest at the top end of the keyboards so that the high notes decay more rapidly than the base notes.

Figure 4. Showing the relationship between key contact changeover and closing and the voltages on C_A and C_B .

Figure 5. Illustrating the complete cycle of U_C and U from depressing the key to releasing it.

Figure 6. Chopper circuit used in the Elektor piano.

Figure 7. Chopper circuit suggested by General Instrument. Although simple and cheap, this circuit has inadequate isolation in the 'off' state.

Figure 8. Complete keying circuit for one octave of the piano.

Table 1. This table gives the values of the discharge resistors R1 to R12 for each octave of the piano. In any one octave R1 to R6 have the same value and R7 to R12 have the same value.

(see table 1).

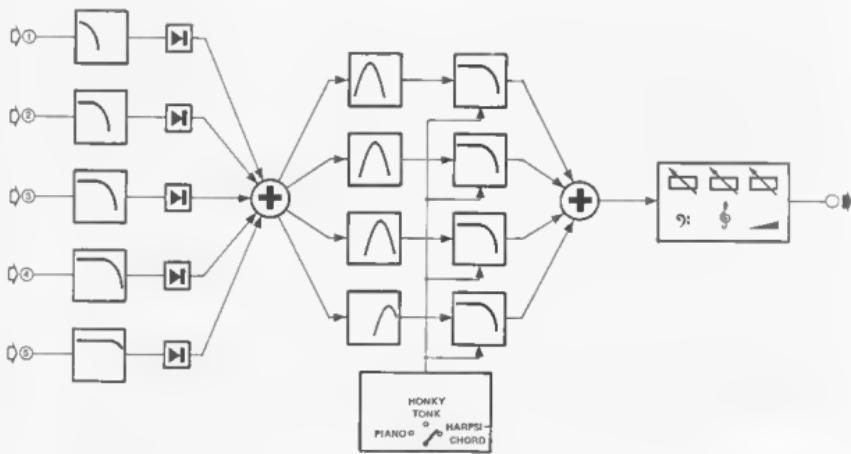
This relatively slow decay continues until the key is released, when the output of comparator $k1$ goes low and T_d turns on. C_b now discharges fairly rapidly through R_g , T_d , and T_e , which simulates the action of the dampers in a conventional piano. However, if the sustain line is connected to zero volts, then T_e is turned off and C_b continues to discharge only through R_h . This simulates the lifting of the dampers by the sustain pedal of a normal piano. The entire output waveform of the envelope shaper is shown in figure 5, on a longer time scale than figure 4.

Chopper circuit

The output of each envelope shaper is fed to a chopper circuit, figure 6, which consists of an emitter-follower to act as a buffer and an electronic switch consisting of one quarter of a 4066 CMOS analogue switch IC. The control input of the switch is driven by the appropriate output of the master tone generator so that the switch 'closes' and 'opens' at the frequency of this signal. When the switch is closed it has a resistance of about 80 ohms and the envelope voltage is allowed through to the output. When the switch is open it has a resistance of several megohms and the envelope voltage is blocked. The output from the switch is thus a squarewave having the same frequency as the control voltage.

Table 1

octave	lowest		highest		R1...	R6	R7...	R12
	note	[Hz]	note	[Hz]	{Ω}		{Ω}	{Ω}
1	c#3	1109	c ⁴	2092	150 k		180 k	
2	c#2	554	c ³	1046	220 k		270 k	
3	c#1	277	c ²	523	330 k		390 k	
4	c#0	139	c ¹	262	470 k		560 k	
5	c#	69	c ⁰	131	680 k		820 k	



age and an envelope the same as that of the envelope shaper output.

This chopper circuit may seem complicated compared with the simple circuit suggested in the General Instruments application notes, which is shown in figure 7. However, this circuit was tested in the Elektor laboratory and was found to have insufficient isolation in the 'off' state, so that signal breakthrough occurred from all notes even with no key depressed, giving rise to an unpleasant background buzzing known as 'beehiving'.

This poorly designed chopper circuit has caused many piano and organ manufacturers to regard the AY-1-1320 with suspicion, which is a pity, since the envelope shaper IC performs its function admirably. Breakthrough in the Elektor circuit, however, is minimal, and signal suppression is further enhanced by muting circuits in the filters, which suppress any signals or noise which are below a preset level. The complete envelope shaper circuit for one octave of the piano is given in figure 8. The outputs of the individual envelope shapers are summed by R25 to R36 and P1 adjusts the overall level for each octave.

Filter circuits

Filtering in the Elektor piano is carried out in three stages. In a conventional piano the harmonic content of the notes varies over the compass of the instru-

ment, low notes having a greater harmonic content than high notes. In the Elektor piano preliminary filtering is carried out by means of five lowpass filters, one for each octave, as shown in the block diagram of figure 9. The filters for the higher octaves have lower turnover frequencies than the filters for the lower octaves, with the result that the harmonic content of the higher octaves is greatly reduced compared to the lower octaves.

The five filter outputs are then fed to diode muting circuits, which suppress any residual signal breakthrough or noise and pass only 'genuine' signals from the keying circuits. The muting circuits are followed by four bandpass filters with different centre frequencies. By feeding each octave in different proportions to two or more of these filters the harmonic structure of every octave can be tailored fairly accurately. For example, the low notes are to have a high harmonic content. This is achieved by feeding a large proportion of the low octave output into the bandpass filter with the highest centre frequency, and relatively smaller proportions into the filters with lower centre frequencies, the result being that the higher harmonics are boosted relative to the fundamental and lower harmonics.

The four bandpass filter outputs are then fed to voicing filters, which provide a choice of piano, honky-tonk or

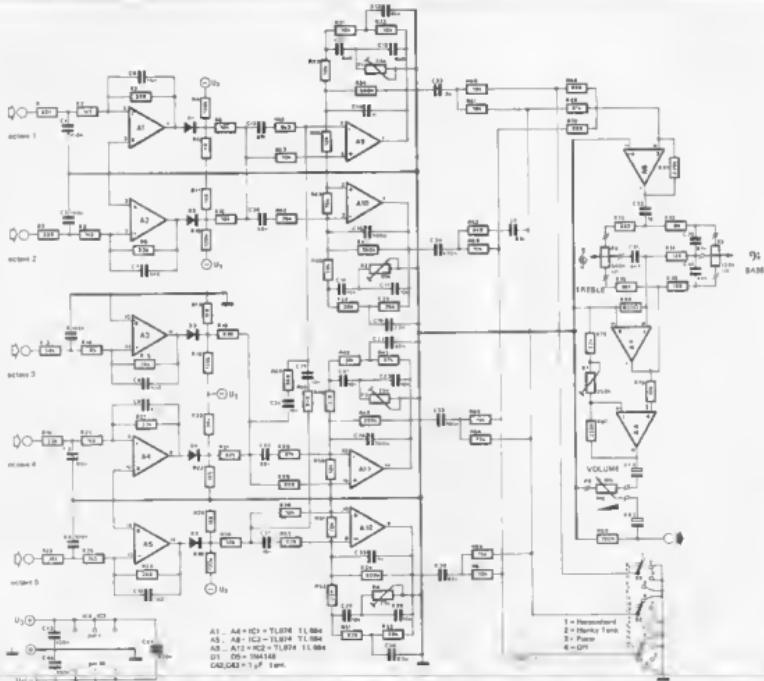
harpsichord sound. Finally, the outputs of the voicing filters are mixed and fed to a preamplifier incorporating tone and volume controls, the output of which can be fed direct to a power amplifier. A soft pedal or expression pedal may also be incorporated into this stage, as will be described later.

Complete filter circuit

The complete circuit of the filters is given in figure 10, all the filters and tone controls being based on Texas TL 074 quad FET opamps.

The five lowpass filters which perform the preliminary filtering are constructed around A1 to A5. The muting circuits at the output of these filters consist of D1 to D5 and their associated resistors. The outputs of A1 to A5, connected to the anodes of these diodes, are at zero volts with no input signal, whilst the cathodes of the diodes are biased to about -0.16 V. This means that the output signals from A1 to A5 must exceed approximately 0.4 V before D1 to D5 will become forward-biased and will allow signals to pass. Any breakthrough or noise signals below this level will be blocked since they will be insufficient to exceed the knee voltage of these diodes.

The four bandpass filters each consist of an opamp with a twin-T selective network in its feedback loop. Each of the five octave outputs is split and fed in



Parts list for figures 10 and 11.

Resistors:

R1,R3 = 68 k
 R2,R5,R6,R11,R14,R17,
 R20,R23,R26,R29 = 1k5
 R4,R10,R16,R22,R28 = 120 k
 R6,R12,R30,R31,R32,R33,R36,
 R37,R43,R50,R56,R57,R60,
 R61,R63,R65,R67,R78,R82 = 10 k
 R7,R9 = 82 k
 R13,R15,R25,R27,
 R38,R39,R40,R42 = 39 k
 R18,R24,R49,R51,
 R52,R53,R55,R79 = 22 k
 R19,R21 = 33 k
 R34 = 560 k
 R35,R58 = 8k2
 R41,R47 = 390 k
 R44,R45,R46,R48 = 27 k
 R54,R71,R80 = 220 k
 R59,R62 = 6k8
 R64,R66 = 15 k
 R68,R69,R70 = 47 k
 R72,R73,R74 = 12 k
 R75,R76 = 3k9
 R77 = 820 Ω
 R81 = 100 k
 P1,P3,P4 = 25 k (22 k) preset
 P2 = 50 k (47 k) preset
 P5 = 100 lin. pot.
 P6 = 500 k (470 k) lin. pot.
 P7 = 250 k (220 k) preset
 P8 = 10 k log. pot.*

Capacitors:

C1 . . . C5,C35,C45,C46 = 100 n
 C6,C13,C33 = 15 n
 C7,C8,C11,C12 = 6n8
 C9,C41 = 4n7
 C10 = 2n2
 C14,C32 = 1 n
 C15,C36,C37,C39,C40 = 47 n
 C16,C17,C21,C22,C27,
 C28,C29,C31 = 10 n
 C18,C26 = 560 p
 C19,C23,C24,C25,C30 = 22 n
 C20 = 68 n
 C34 = 470 n
 C38 = 1 μ
 C42,C43 = 1 μ tantalum
 C44 = 220 n

Semiconductors:

D1 . . . D5 = 1N4148
 IC1,C2,C3 = TL074 (Texas),
 XR4212 (Exar)

Miscellaneous:

S1,S2,S3 = single-pole on-off switch

* If an 'expression' pedal is required, P8 should be pedal-controlled. Alternatively, if a 'soft' pedal is required, a 10 k preset should be included between P8 and C42, with a pedal-operated normally-closed switch in parallel with this preset.

11

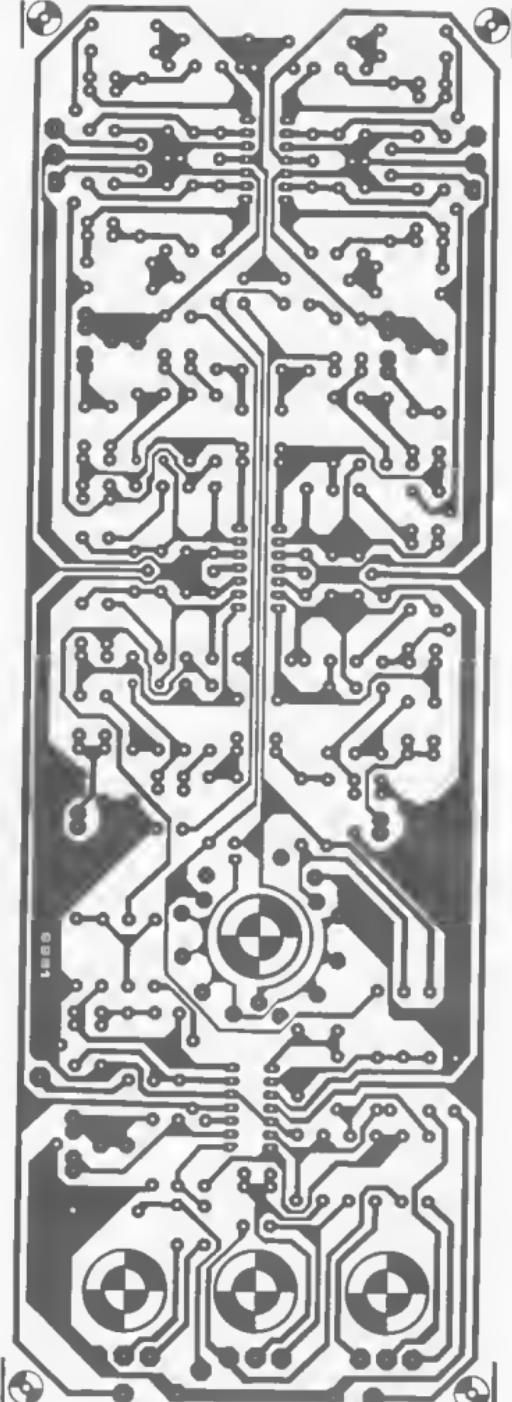
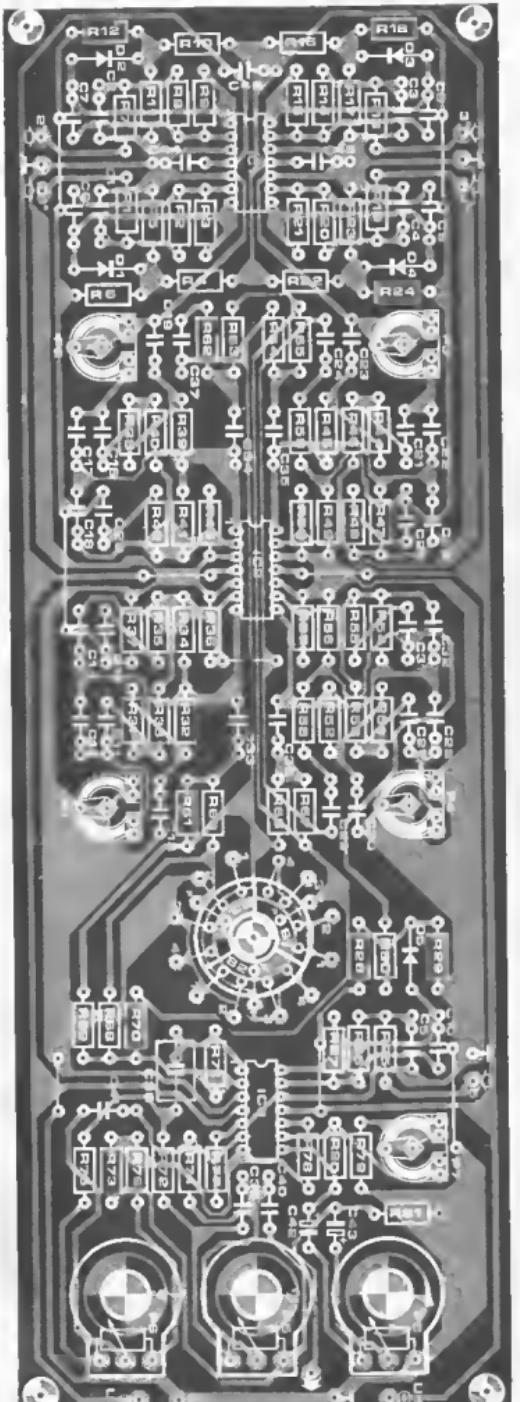


Figure 11. Printed circuit board and component layout for the filter section. (EPS 9981).



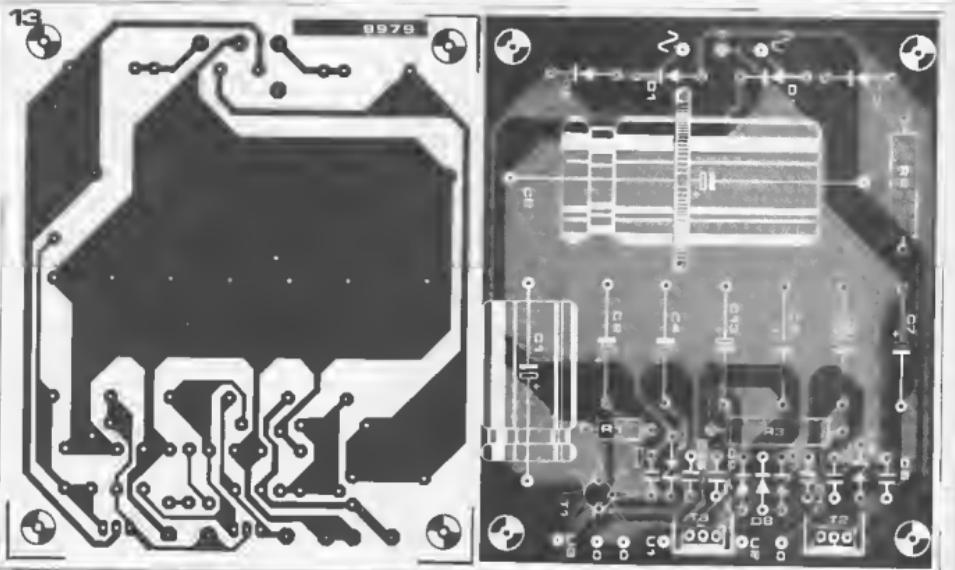
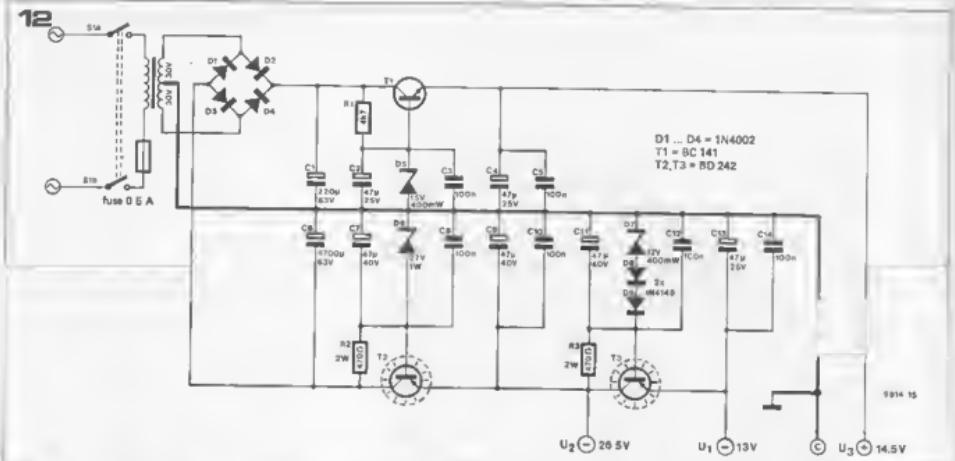


Figure 12. Power supply for the complete piano.

Figure 13. Printed circuit board and component layout for the power supply. (EPS 9979).

Figure 14. Printed circuit board and component layout for one octave of the keying circuit. (EPS 9914).

Parts list for figures 12 and 13.

Resistors:

R1 = 4k7
R2,R3 = 470 Ω/2 W

Capacitors:

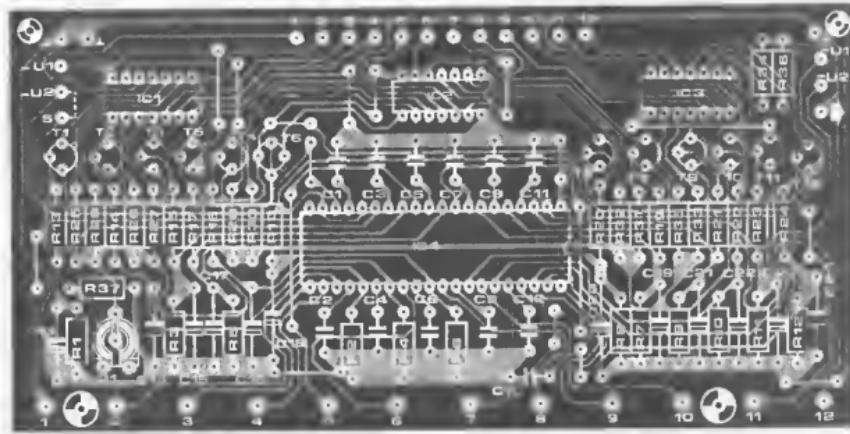
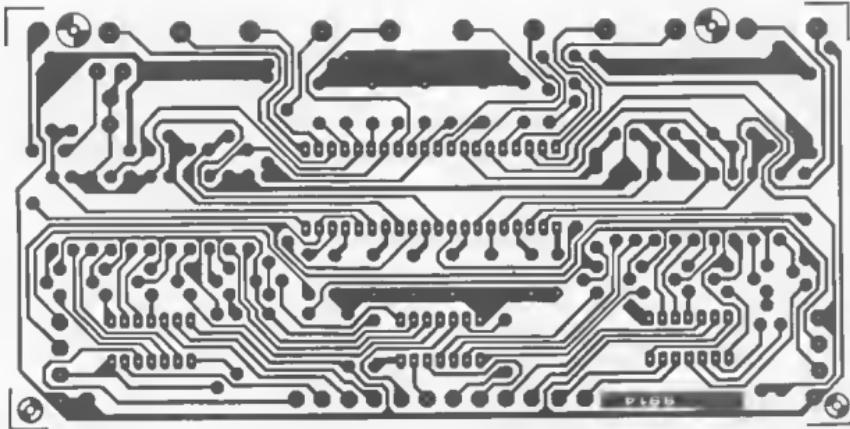
C1 = 220 µF/63 V
C2,C4,C13 = 47 µF/25 V
C3,C5,C8,C10,C12,C14 = 100 n
C6 = 4700 µF/63 V
C7,C9,C11 = 47 µF/40 V

Semiconductors:

D1 ... D4 = 1N4002
D5 = zener 15 V/400 mW
D6 = zener 27 V/1 W
D7 = zener 12 V/400 mW
D8,D9 = 1N4148
T1 = BC 141
T2,T3 = BD 242

Miscellaneous:

Tr = mains transformer with
2 x 30 V/500 mA secondaries or
30-0-30/500 mA sec.
S1 = double-pole on/off mains switch



Parts list for figures 8 and 14.

Resistors:

R1 ... R12 = see text and table 1
 R13 ... R24 = 47 k
 R25 ... R36 = 6k8
 R37 = 100 Ω
 P1 = 10 k preset

Capacitors:

C1 . . . C12 = 470 n polycarbonate
or polyester
C13 . . . C24 = $2\mu 2/35$ V

Semiconductors:

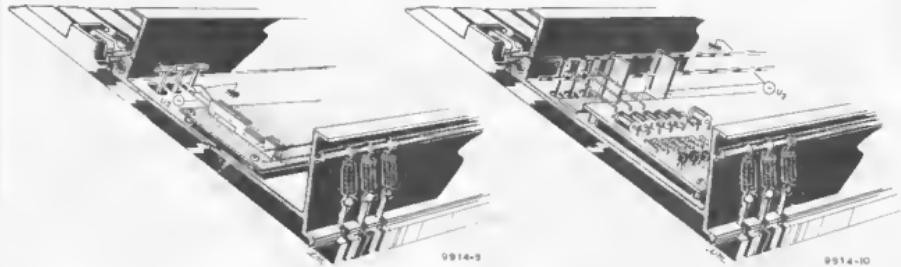
IC1 . . . IC3 = 4066
IC4 = AY-1-1320
T1 . . . T12 = TIP

the piano voicing, which is carried out by ear. Preset P1 on each envelope shaper board allows the overall output level from each octave to be adjusted, partly to compensate for variations in the characteristics of the envelope shaper ICs and partly to allow the loudness of each octave to be adjusted to that of a conventional piano.

Presets P1 to P4 in the bandpass filters determine the tone of the piano, which can be varied from soft and muffled to a hard, steely sound. This, of course, is a matter of personal taste. The voicing adjustments should, of course, be carried out with the tone controls in the flat position. Preset P7 should be used to set the gain of A3 to suit the power amplifiers.

fier used, e.g. so that with the volume control at maximum the output is just on the point of clipping when a complex chord is played *fortissimo*. Finally, the soft pedal preset, if fitted, should be used to give the desired degree of muting when the soft pedal is pressed. As a final comment to avoid complaints from the musical purists, it should be noted (no pun intended) that the piano does not give an accurate simulation of the amplitude dynamics of a harpsichord. The strings of a harpsichord are plucked by quills rather than struck, and the loudness of a note is determined largely by the tension at which the quill releases the string, rather than by key velocity.

15

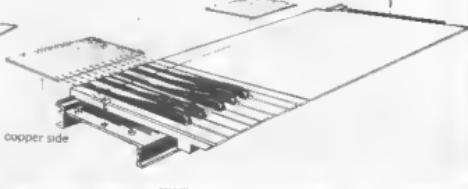


16

copper side



component side



Bulk component list for 5-octave piano (including master tone generator)

Resistors:

value:	number:
100 Ω	5
820 Ω	1
1 k	1
1k5	10
2k2	2
3k9	2
4k7	1
6k8	62
8k2	2
10 k	19
12 k	3
15 k	2
22 k	9
27 k	4
33 k	2
39 k	8
47 k	63
68 k	2
82 k	2
100 k	1
120 k	5
150 k	6
180 k	6
220 k	9
270 k	6
330 k	6
390 k	8
470 k	6
560 k	7
680 k	6
820 k	6
1 M	1
470 Ω/2 W	2
preset 10 k	5
preset 25 k (22 k)	3
preset 50 k (47 k)	1

value:	number:
preset 250 k (220 k)	1
potentiometer 10 k log	1
potentiometer 100 k lin.	1
potentiometer 500 k (470 k) lin.	1

Capacitors:

value:	number:
27 p	1
47 p	1
560 p	2
1 n	2
2n2	1
4n7	2
6n8	4
10 n	8
15 n	3
22 n	5
47 n	7
68 n	1
100 n	14
220 n	1
470 n	61
1 μ	1
1 μ tantalum	2
2μ/35 V	60
47 μ/25 V	3
47 μ/40 V	3
220 μ/63 V	1
4700 μ/63 V	1
trimmer 45 p	1

Semiconductors:

type:	number:
4024	12
4049	3
4066	15
AY-1-0212, M 087	1

	5
AY-1-1320	5
TL074, XR 4212	3
TUP	60
BC 141	1
BD 242	2
1N4002	4
1N4148	7
zener 12 V/400 mW	1
zener 15 V/400 mW	1
zener 27 V/1 W	1

Miscellaneous:

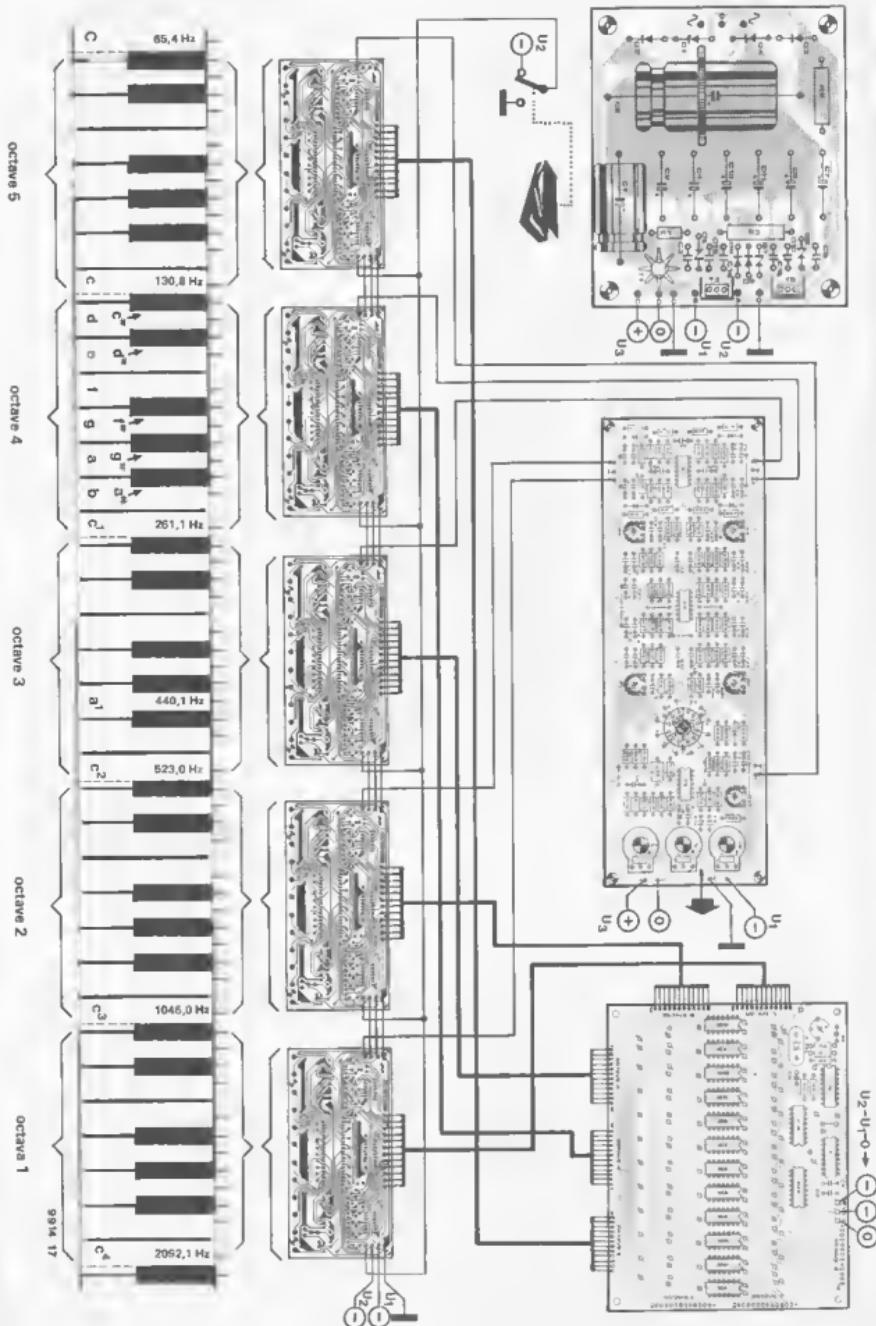
crystal 1 MHz
 mains transformer 2 x 30 V/500 mA
 3 x SPST switch
 double pole on/off mains switch
 5-octave C-C keyboard

Figure 15. The key contacts may be ready-assembled or home-made. In either case the moving contact is soldered to the keying circuit p.c. board whilst the fixed contacts are connected to ground and -26.5 V bus-bars.

Figure 16. Depending on the type of keyboard used, the keying circuit board may be mounted either way up to facilitate soldering to the contact tails. Depending on which way it is mounted it may be necessary to transpose the inputs and R1 to R12.

Figure 17. Wiring diagram for the complete piano. Connections between the master tone generator and the keying circuits may be made using ribbon cable.

17



temperature-controlled soldering iron

Since the days when soldering irons were heated up on gas rings, the design of this virtually indispensable piece of equipment has come a long way. There is now a wide variety of different types of iron available, allowing power rating as well as size, shape and composition of the bit to be selected to suit a particular application. Despite this plethora of different irons, it is nonetheless possible to discern two basic categories, namely continuous heat and temperature-controlled soldering irons. With the former type, the heating element is connected continuously to the supply, with the result that the iron tends to run very hot when not being used.

This means that the first joint made after the iron has been left standing may be too hot, thereby incurring the risk of a bad joint or of damage to delicate components. If one attempts to combat this problem by using a lower power iron, there is the danger that, under heavy load conditions, it may be unable to supply sufficient heat and will make a dry joint. A further disadvantage of continuous heat irons is that their tendency to overheat shortens the effective life of the bit and causes a reduction in the heating capability of the iron.

Temperature-controlled irons on the other hand suffer from none of these drawbacks. The only reason that they have not completely replaced continuous heat types is the fact that they cost much more. However, with the current trend towards ever smaller and more sensitive components, the decision to purchase a temperature-controlled iron may well prove a worthwhile long-term investment (particularly if one considers saving the cost which results from building the control unit oneself).

Thermostatically controlled soldering irons must not only be able to maintain a constant bit temperature (to within a few degrees Centigrade), it must also be possible to vary the soldering temperature to suit different requirements. Designing a suitable control unit, which both meets the above conditions and yet is a reasonable financial proposition for the amateur constructor, is no easy matter. However, the circuit described in this article adequately fulfills all the

Electronic temperature-controlled soldering irons offer a number of advantages over continuous heat types: delicate components are protected against thermal damage; they permit the use of higher wattages, thereby eliminating the danger of dry joints when working under heavy load conditions; and finally they increase the life of both heating element and bit. The following circuit is for a thermostatic control unit, which is both easy to build and uses standard components. Suitable soldering irons containing a built-in heat sensor are readily available from a number of different manufacturers.

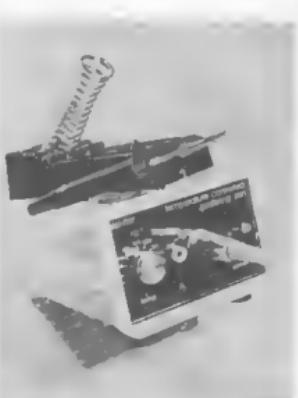
desired design criteria at a price which is roughly halfway between the cost of a conventional continuous heat iron and that of a commercially available temperature-controlled model. The control unit is designed for use with a readily available soldering iron incorporating a heat sensor in the shaft adjacent to the tip of the bit.

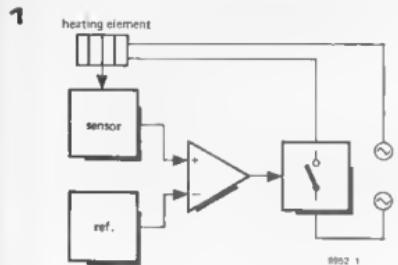
Electronic control unit

The principle of the electronic thermostatic control unit is illustrated in the block diagram shown in figure 1.

A sensor mounted in the element as near as possible to the bit tip provides a voltage which is proportional to the bit temperature. This voltage is then compared with a (variable) reference voltage on the other input of a comparator, the output of which is used to control a switch which regulates the flow of current to the heating element in the iron. Thus, when the sensor voltage is lower than the reference value, the switch is closed, current flows to the heating element and the bit temperature rises; once the desired temperature is reached, the comparator output changes state, opening the switch and thereby cutting off the flow of current to the heating element. The bit temperature then falls until the threshold voltage of the comparator is again reached and the control switch is opened. In this way the temperature of the bit can be maintained within a certain fixed range. The amount of hysteresis between a change in temperature and the corresponding change in sensor voltage is determined by the thermal inertia of the sensor itself and the thermal conductivity of the bit (which in turn is determined by the size and composition of the bit).

The deviation from the nominal bit temperature as a result of the hysteresis of the control system is illustrated in figure 2. As can be seen, the bit temperature oscillates about a preset nominal value; the steepness of the rising edge of the triangular waveform is largely determined by the output power of the heating element, and that of the falling edge by the rate at which heat is lost to the atmosphere, solder, p. c. b.





etc. In practice however, the bit temperature only deviates very slightly from the desired nominal value, so that it is in fact possible to speak of an average working temperature of the iron.

As far as the choice of heat sensor is concerned, various possibilities come into consideration. The firm Weller, for example, manufacture a heat sensor which utilises an unusual property of magnetic materials. Above a certain temperature, known as its Curie point, a ferromagnetic material loses the property of magnetism. The bit of a Weller iron contains a slug of magnetic material, which, when the iron is cold, attracts a magnet. This in turn closes a switch and applies power to the heating element. When the temperature of the bit reaches the Curie point, the slug ceases to attract the magnet, causing the switch to be opened. The only disadvantage of this system is that a different bit containing a ferromagnetic slug with the appropriate Curie point is needed to change the soldering temperatures.

Other manufacturers employ heat sensors consisting of a thermocouple or of an NTC- or PTC thermistor, usually as part of a bridge circuit. One branch of the bridge is formed by a variable resistor with which the bridge is balanced. In practice this means that the temperature range of the bit is determined by the range of the resistor.

Of the above-mentioned types of sensor, the thermocouple represents the best choice. The reasons for this are clear when one compares it with temperature-dependent resistors. Firstly, the dimensions of the thermocouple are smaller than those of an NTC or PTC thermistor, which means that it is easier to mount close to the tip of the bit, and also that, because of its reduced mass, it responds more quickly to changes in temperature. The response of a thermocouple (voltage as a function of temperature) is, as figure 3 clearly shows, linear over a wide range of temperatures. NTC- and PTC thermistors, on the other hand, exhibit a far less linear characteristic. Furthermore, a thermocouple has no quiescent current flow to speak of, and hence will not generate any heat itself. The final point in its favour is the lower cost of thermocouples, a not insignificant factor

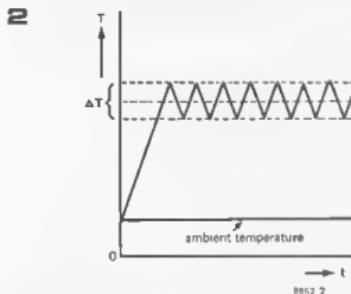


Figure 1. Block diagram of an electronic thermostatic control unit for soldering irons. The voltage from the heat sensor is compared with a variable reference voltage. The output of the comparator controls a switch which is used to turn the flow of current to the heating element on and off.

Figure 2. The response of a typical thermostatic control unit. The temperature first climbs to the desired (preset) value. However, once it reaches this value the temperature continues to rise, due to the inherent hysteresis of the system, before the interruption of current to the heating element begins to take effect. Similarly, when the temperature has fallen to the nominal value, it will continue to drop slightly before the renewed flow of current to the heating element can begin to push the temperature back up. Thus the actual bit temperature of the iron tends to oscillate about the nominal 'controlled' temperature. However, in practice these variations in temperature are sufficiently small not to significantly effect the performance of the iron, which remains at a more or less constant 'average' temperature.

when temperatures of the order of 400°C are involved.

The Elektor control unit

In view of the above-mentioned points, an iron which was both readily available and which incorporates a thermocouple as heat sensor was taken as the starting point of the Elektor control unit. Several manufacturers in fact distribute suitable soldering irons without the accompanying control unit. For example, the firm Antex produce a 30 W soldering iron (the CTC) which includes a thermocouple, as well as a 50 W model (XTC) which should be available shortly. Ersa are another company who have a suitable 50 W iron (TE 50).

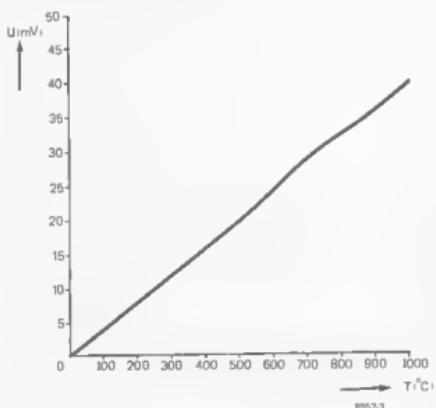
In order to ensure the complete reliability of the Elektor control unit, it was in fact sent to Antex for assessment. Their verdict was summarised as follows: 'The performance of the sample tested should be perfectly adequate for the Home Constructor'. Furthermore, the control unit can also be used with soldering irons from most of the other manufacturers, even if they contain NTC- or PTC thermistor sensors, although in that case certain changes will have to be made to the circuit. Without entering into the theoretical details, it should be noted that different combinations of materials can be used to construct thermocouples, and that each will deliver a different output voltage for a given temperature. For their CTC and XTC models, Antex use a K-type thermocouple, which is composed of nickel-chrome and nickel-aluminium. The response shown in figure 3 was obtained using this type of thermocouple.

Circuit diagram

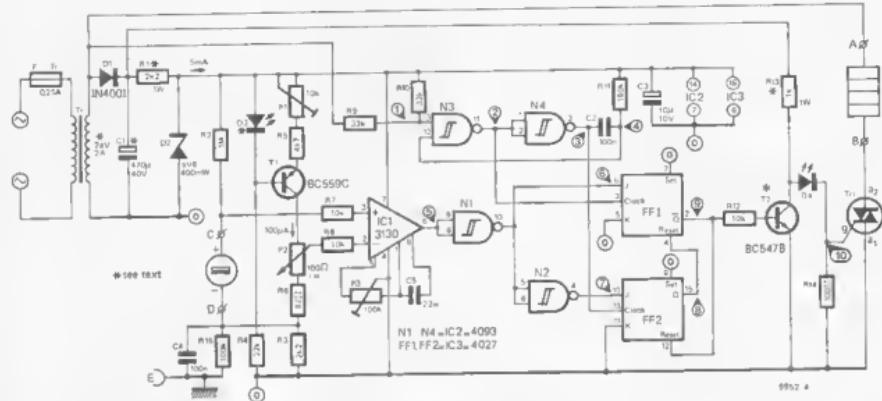
The complete circuit diagram of the thermostatic control unit is shown in figure 4. Despite the small number of components used, the operation of the circuit is somewhat involved, and for this reason figure 5, which contains an overview of the waveforms found at the test points shown, is included to facilitate explanation.

The first problem which arises is the

3



4



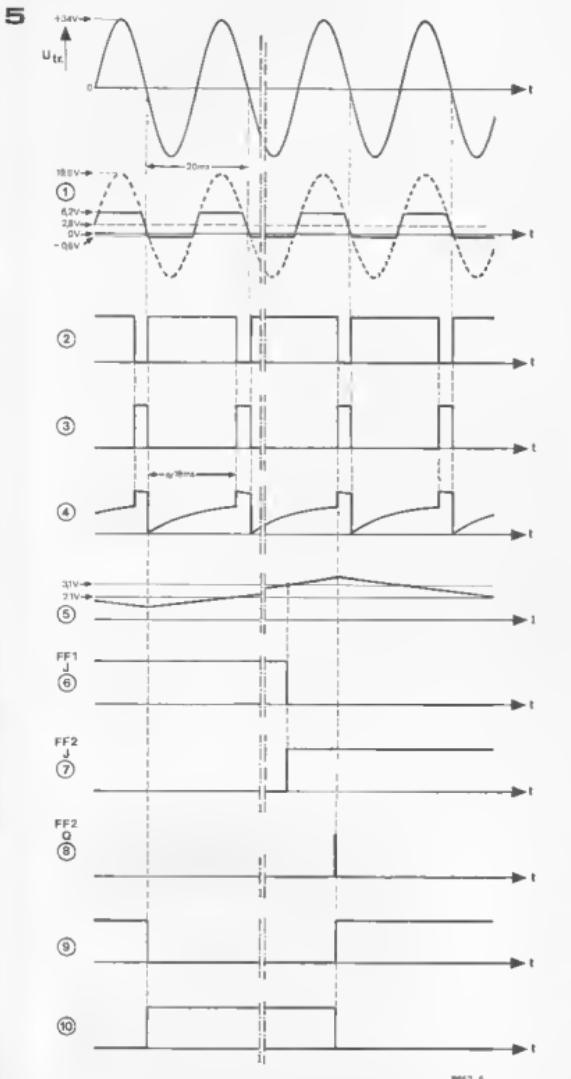
choice of switching element to regulate the flow of current to the iron. The use of a relay involves several drawbacks (contact burning, contact bounce etc.) which can be avoided by employing an electronic switch such as a triac. An additional advantage of a triac is that the switching point can be controlled with a high degree of accuracy, i.e. in order to reduce the switch-on surge current and r.f. interference to a minimum, the triac can be triggered at the zero-crossing point of the AC waveform. This is in fact the arrangement adopted in the circuit described here.

R4, D3, T1 and the emitter resistors of T1 form an adjustable constant current source. D3 is a LED used to set the DC base bias voltage of T1, but since it draws very little current it will hardly light up at all. The advantage of this somewhat unusual approach is that the LED possesses the same temperature coefficient as T1, hence the stability of the current source is unaffected by variations in temperature. This is only true, however, if the ambient temperature of the circuit does not rise too far above normal room temperature, since in that case the temperature coefficient

of the LED will cease to match that of T1. Thus, if when the circuit and transformer have been mounted in a case, the temperature should rise by more than 30°C, D3 should be replaced by an 8k2 resistor. This step will obviously be necessary if the soldering stand is to be mounted on top of the controlunit case. The current through P2 and R6 can be varied by means of P1. P2 determines the amplitude of the reference voltage at the inverting input of IC1. The thermocouple is connected across the non-inverting input of IC1 and the junction of R3/R6. Thus the voltage

Figure 4. The complete circuit diagram of the Elektor thermostatic control unit. The modifications needed for the 40 V version are listed in table 1.

Figure 5. Pulse diagram of the various signals obtained at the test points shown in figure 4.



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difference at the inputs of the comparator equals the difference between, on the one hand, the voltage dropped across R_6 plus the resistance of P_2 , and on the other hand, the voltage developed by the thermocouple. That is to say, it virtually equals the thermocouple voltage.

If the soldering iron is cold, the thermocouple voltage is very small, so that the output of $IC1$ is low. When the temperature of the iron rises, the thermocouple voltage, and hence the voltage difference at the comparator inputs, also rises, until the output of the

comparator swings high.

$IC1$ is followed by a Schmitt trigger, the output of which goes low when the input exceeds approx. 3.2 V, and high when it falls below roughly 2.1 V. This arrangement could be used directly to control the triac were it not that we have to first ensure that the load is switched at the zero-crossing points of the transformer voltage. To achieve this, one or two extra provisions are required. The transformer voltage (U_{tr} in figure 5) is connected to the input of $N3$ via a potential divider, R_9 and R_{10} , one end of which is connected to the stabilised

5.6 V supply rail. This means that the voltage at point 1 (the input of $N3$) exactly tracks the transformer voltage, whilst remaining 2.8 V 'up' on the latter (see figure 5). The portion of waveform above 6.2 V and below -0.6 V is shown as a dotted line, since CMOS Schmitt triggers contain clamping diodes which protect the inputs from voltages which exceed these limits.

The advantage of the 2.8 V positive offset is apparent from figure 5, since it means that when the transformer voltage is zero, the voltage at point 1 is 2.8 V; since the Schmitt trigger changes state at the threshold values of 2.1 V and 3.1 V, we can say that, in spite of the hysteresis, it is only triggered around the zero-crossing point of the transformer waveform (the small deviation from the ideal switching point of exactly 0 V can be eliminated by making R_9 variable and using a scope to adjust it to the correct value; in practice, however, this small error is of little significance and does not materially affect the operation of the circuit). When both inputs of $N3$ are high (i.e. greater than 3.1 V), the output is low, and since $N4$ is connected as an inverter, its output will be high, with the result that $C2$ will be discharged. If point ④ then goes low, since $C2$ is still uncharged, point ④ will also go low, causing $C2$ to charge up via R_{11} . The time constant of $R_{11}/C2$ is 18 ms; shortly before this time is reached the voltage at pin 12 of $N3$ will have reached the logic '1' threshold and since, at that moment, pin 13 has once more been taken high, the output of $N4$ is also returned high. Since capacitor $C2$ is already charged, the voltage across it would continue to rise, but for the clamping diode in $N3$. The capacitor is rapidly discharged (figure 5 ④), and a new cycle begins.

The signals at points ④ and ⑧ form the clock signals for flip-flops $FF1$ and $FF2$. The J-inputs of these flip-flops are connected to points ④ and ⑧, where the voltage is determined by the temperature of the iron, whilst the K-inputs are connected to ground. Only when the J-inputs are high can the clock pulses have any effect and change the state of the flip-flops. Since the voltage at point ④ is an inverted version of that at point ⑧, when the former goes low the first positive-going edge at point ④ will take the Q output of $FF1$ (point 9) low, causing $T2$ to turn off and the triac to be triggered. The soldering iron then begins to heat up, so that the voltage at point ④ rises until it reaches the trigger threshold of $N1$. When that happens $N1$ changes state, taking point ④ low and point ⑧ high; the next positive going pulse at point 3 will take the Q output of $FF2$ high and reset $FF1$, thereby taking point ④ high and resetting $FF2$. Thus $T2$ is turned on and the triac turned off, interrupting the flow of current to the heating element in the iron. The temperature of the iron will fall until the lower threshold value of

Parts list

Resistors:

R1 = 2k2 1W
 R2 = 1M
 R3 = 2k2
 R4 = 22 k
 R5 = 4k7
 R6 = 82 Ω
 R7, R8, R12 = 10 k
 R9, R10 = 33 k
 R11 = 180 k
 R13 = 1 k 1W
 R14 = 100 Ω
 R15 = 100 k

P1 = preset potentiometer 10 k
 P2 = potentiometer 100 k linear
 P3 = preset potentiometer 100 k

Capacitors:

C1 = 470 μ /40 V
 C2 = 100 n
 C3 = 10 μ /10 V
 C4 = 100 n
 C5 = 22 n

Semiconductors:

D1 = 1N4001
 D2 = 5V6/400 mW
 D3 = LED red
 D4 = LED
 T1 = BC 558C
 T2 = BC 547B
 Tri = 2 A/100 V (or 4 A/400 V)
 IC1 = 3130
 IC2 = 4093
 IC3 = 4027

Miscellaneous:

transformer 24 V/2 A
 fuse 0.25 A slow blow
 soldering iron with built-in heat
 sensor, e.g. Antex type CTC or
 XTC
 soldering stand.

N1 is reached, whereupon a new cycle will begin.

Those phases during which current is fed to the iron (i.e. when the triac is conducting) are indicated by LED D4 lighting up.

The waveforms shown in figure 5 do not exactly coincide with those obtained in practice, since the noise at the inputs of IC1 (which in no way affects the performance of the circuit) has, for the purpose of clarity, been omitted from the diagram.

Construction

Figure 6 shows the track pattern and component layout of the p.c.b. for the circuit of figure 4.

Constructing the control unit should not present any major problems. Connection points A . . . E marked on the board correspond to those shown in figure 4, and are in fact the holes for connections to the soldering iron.

Figure 7 shows the DIN-plug of the Antex CTC soldering iron with details of the correct pin connections and colour of the leads.

In principle the triac should require no heat sink; however if the circuit is mounted in a small case and the iron is operating under heavy load conditions, then the use of a heat sink is strongly recommended (not to mention ventilating the case). In fact every effort should be made to prevent any rise in the ambient temperature of the circuit, since, as was already mentioned, this will have an adverse effect upon the temperature coefficient of the constant current source.

Figure 6. Track pattern and component layout of the p.c.b. for the circuit of figure 4. (EPS 9952).

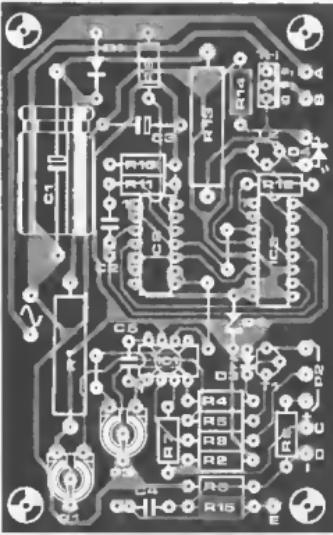
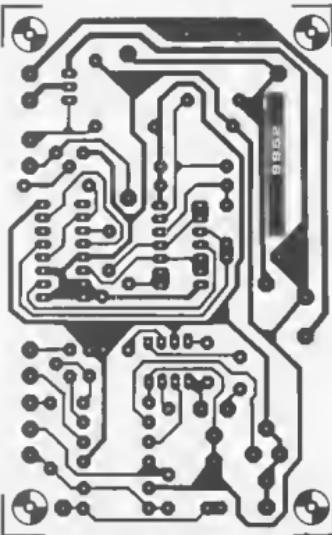
Figure 7. The Antex soldering iron is fitted with a DIN-plug. Pins A . . . E correspond to connection points in the circuit of figure 4. Pin E is shown as a ground point and connects to the metal body of the iron.

On no account should the 0 V rail of the control circuit be connected to mains earth, although it is permissible to earth a metal case, if one is used.

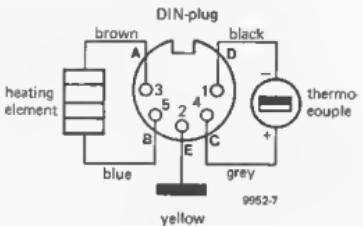
Table 1.

40 V-Version

U_{tr}	40 V/1 A
R1	4k7, 3 W
C1	470 μ /63 V
R13	2k2, 3 W
T2	BC 546



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The photo shown on the first page of this article is a prototype model of the Elektor control unit. For exhibition purposes the unit was housed in perspex. The soldering stand shown in this photo is not particularly suited for low power irons, since the contact between the iron and the metal rings leads to considerable heat loss and hence to the iron being switched on and off with excessive frequency. Soldering stands which avoid direct metal-to-metal contact with the iron should be given preference. These can be bought separately from most electronics shops.

Adjustment procedure

The setting up procedure for the control unit is as follows:-

Firstly, with the soldering iron disconnected, the inputs of IC1 are shorted together. The offset voltage is then reduced to a minimum by adjusting P3 until D4 either just lights up or is just

extinguished (depending upon which state it assumes when power is applied). Next, the short is removed and the wiper of P2 is turned fully towards R6 (anticlockwise). The soldering iron is then plugged in and the tip is held against a length of solder. Although solder melts at approx. 189°C (60/40 alloy), at around 185°C it exhibits a 'plastic' consistency. By very gradually adjusting P1, it is possible to set the temperature of the iron such that the solder is in this plastic state, just on the point of melting (185°C). P1 should be adjusted in small steps, always allowing the temperature of the iron to stabilise before testing it against the solder and performing another adjustment. By means of P2, it is then possible to vary the temperature of the iron between 185°C and approx. 400°C. P2 can be calibrated using the following equation:

$$T = 185 + \frac{P2}{82} \times 185^\circ\text{C} \quad (P2 \text{ is in } \Omega)$$

In conclusion

As was already mentioned, the prototype model of the control unit was designed for use with the CTC or XTC soldering iron from Antex. However it can also be used with other types of iron, particularly if they are provided with a thermocouple heat sensor. If this is the case, and if the iron operates off 24 V, then it can be connected direct to the Elektor control unit. In the case of an iron with the same operating voltage but which employs a different sort of sensor, the situation is a little more complicated. With a PTC thermistor, D3 and D4 should be omitted, T1 replaced by a wire link between the emitter and collector connections, and the value of R2 altered accordingly. The same procedure holds good for irons incorporating an NTC thermistor, with the exception that R2 and the NTC should be transposed.

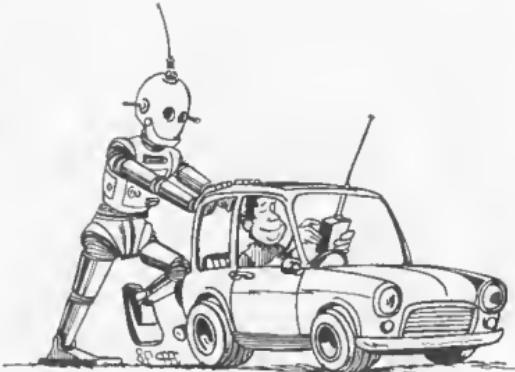
In the case of an iron employing a thermocouple and operating from a 40 V supply, the modifications shown in table I should be adopted.

The above-described control unit is thus suitable for use with a wide variety of different types of soldering iron, and represents considerable saving in cost over commercially available models.

The final point worth noting is that the circuit can not only be used to regulate the temperature of soldering irons, but can be adapted for a number of other applications requiring a thermostatic control unit, such as, e.g. clothes irons, ovens, central heating etc.



car start booster



As all car owners know, during the winter one has to be especially careful to ensure that the battery voltage is not allowed to fall too low, otherwise there is the very real danger of the car failing to start. The main reasons for this are firstly, that the low temperature of the electrolyte increase the effective internal resistance and hence reduces the capacity of the battery. At -20°C this can be as little as 40% of the capacity at 25°C . This means a lower discharge voltage for the same discharge current and therefore that it is easier to drain the battery completely flat under low temperature conditions. Secondly, the low temperature increases the viscosity of the engine oil, making it more difficult for the starter motor to turn the crankshaft. Thus, in winter, the starter motor draws more current from the battery than in summer. A further obstacle is that the relatively low temperature of the air-fuel mixture from the carburettor means that it is more difficult to ignite.

When the ignition key is turned to start the car, the primary winding of the ignition coil is connected via the contact breaker to the battery. However, the lower discharge voltage of the battery when operating at low temperatures means that the current flowing through the primary winding will likewise be smaller than normal. Thus, when the contact breaker opens (at the end of the compression stroke), a smaller voltage is induced in the secondary winding of the ignition coil. The result is that a smaller voltage is applied to the spark plugs, which are being asked to ignite a colder-than-normal mixture. Hardly surprising therefore that one encounters problems when starting the car under cold conditions.

The circuit

It should be clear from the above explanation that one of the ways of improving the starting performance of

Thanks to present-day low prices for nickel-cadmium batteries, it is now an economic proposition to construct a car start booster — an accessory which can prove extremely handy on cold winter mornings.

a car would be to temporarily increase the ignition voltage applied to the spark plugs. This is the basic principle of the car start booster, the circuit diagram of which is shown in figure 1.

S_1 represents the ignition switch; during a normal 'cold start' when the ignition key is turned contact I_1 is first connected to the battery, so that with the contact breaker closed, current flows through the primary winding of the ignition coil. Turning the ignition key further to the right energises the relay, thereby supplying current to the starter motor which turns the flywheel. At the end of the compression stroke the contact breaker opens and the voltage induced in the secondary winding of the ignition coil causes the spark plug to fire. In the modified 'assisted-start' version of the circuit a second relay situated between the ignition switch and ignition coil is energised at the same time as the starter relay. This second relay is used to temporarily switch two Ni-Cad batteries in series with the car battery, thereby increasing the voltage dropped across the primary winding of the ignition coil. The result is obviously a higher current through the primary of the ignition coil, more energy is stored in the resulting magnetic field, and that field collapses a greater voltage is induced in the secondary, voltage induced in the secondary.

Once the engine starts, the ignition key is turned back to the left (normally it is spring-assisted), the relay drops out and normal battery voltage appears across the ignition coil. The Ni-Cad cells are then recharged via R_1 and R_2 . The value of these two resistors depends upon the maximum permissible charge current. Sintered-electrode Ni-Cad cells should be used, since for short periods the discharge current reaches around 4 A.

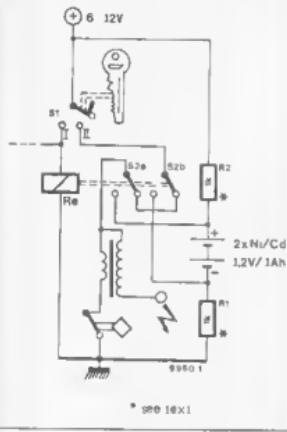
Figure 1. A relay, two Ni-Cad cells and two resistors are required for the 'car start booster'.

Figure 2. This sketch illustrates how the various components are added to the existing car electrical system.

Construction

The relay, the Ni-Cad batteries and the resistors are best fitted near the original

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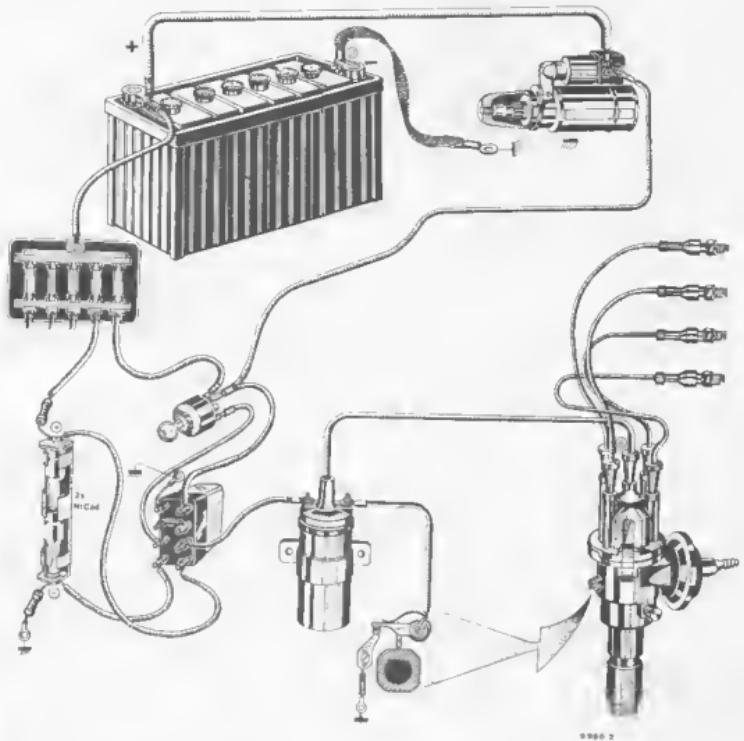
system. The various interconnections are illustrated in the drawing of figure 2. At this stage a few constructional tips would not go amiss. First of all, the lead into which the two relay contacts should be inserted can easily be found working back from the ignition coil. The coil has three external connections; the middle connection, which is protected by a rubber cap, goes to the distributor, and since it carries extremely high voltages, should be left well alone.

Of the two other leads one goes via the contact breaker to the chassis, and the other to the ignition switch in the dashboard. The latter lead is the one that is wanted. The cable should be cut, and each of the ends connected to one of the changeover contacts of the relay. The normally-closed contacts of the relay should be joined together. The Ni-Cad batteries are then connected between the two (normally-open) remaining contacts (taking care to ensure they are the right way round!).

A tap can then be taken from the starter relay lead to the new relay. Thus the coil of the relay is connected between the tap and ground. Mounting the resistors is no problem. R2 for example, can be mounted in the fusebox between the accessory fuse and a connection to the anode of the Ni-Cad batteries. R1 can simply be mounted next to the relay and connected between the appropriate contact of S2b and the earth connection of the relay coil.

If desired, the double-pole changeover relay can be replaced by a normal manually-operated DPDT switch which is mounted on the dashboard and switched on when starting the engine. Although this starter aid should satisfactorily resolve some problems caused by cold weather, it should not be regarded as an excuse to forget about the battery capacity altogether! That is to say, it will be of little help if, for example, one leaves the lights on all night.

22



APPLIKATOR

complex sound generator

The 'complex sound generator' recently introduced by Texas Instruments is intended for generating sound effects. This 28-pin IC, the SN76477N, is one of the first linear 2^2 L chips. A wide range of applications is suggested by TI: alarm indicators, timers, sound effects in toys, TV-games, etc.

The internal block diagram of the SN76477N is shown in figure 2, together with some external components. The 'complex sound' produced by the chip is determined by two analogue voltages (pitch and external VCO control), eight logic levels and a handful of fixed resistors and capacitors. Three basic signals are generated by a 'Super Low Frequency Oscillator' (SLF), a Voltage Controlled Oscillator (VCO) and a noise generator.

Supply voltage regulation is also incorporated in the IC, although this is not always required: the user has the option of applying either a stabilised 5 V supply to pin 15 (U_{REG}) or an unregulated 7.5 to 9 V supply to pin 14 (U_{CC}). In the latter case, the internal regulator will not only power the chip itself but can also deliver up to 10 mA (at 5 V) from pin 15.

Logic levels are TTL- and CMOS-compatible, logic '1' being defined as more than 2 V (nominally 5 V) and logic '0' being zero volts. The various sections of the block diagram will now be described in greater detail.

SLF (Super Low Frequency) oscillator

This oscillator is intended for use in the very low frequency range (0.1 to 30 Hz), but it will operate at frequencies up to 20 kHz. This may prove useful in some specific applications. The generator produces two output signals: a square-wave with a 50% duty-cycle (fed to the mixer) and a triangle-wave which can be used to sweep the VCO.

The frequency (f_S) of the SLF is determined by the external components R_S and C_S :

$$f_S = \frac{0.64}{R_S \times C_S} \text{ (approx.)}, \text{ where}$$

f is in Hz, R in $\text{M}\Omega$ and C in μF .

VCO (Voltage Controlled Oscillator)

The output frequency of the VCO can be varied by means of a control voltage. This control voltage can be derived from the SLF or, alternatively, an external 'Pitch Control voltage' (U_P) can be applied to pin 16. The logic level at the 'VCO select' input (pin 22) determines which one of these control voltages is applied to the VCO. Logic '0' at the VCO select input enables the Pitch Control input; a logic '1' causes the output of the SLF oscillator to be passed to the VCO control input. When the Pitch Control input is enabled, increasing the control voltage U_P causes the frequency of the VCO to decrease. In some cases it may prove useful to have two external Pitch Control inputs. The second input may then be obtained by omitting C_3 and using pin 21 for Pitch Control — the SLF then merely serves as an input buffer.

The frequency of the VCO can be varied over a 1 : 10 range by means of the Pitch Control voltage (U_P). The low end of the range is set by the values of R_V and C_V , as follows:

$$f_{V,MIN} = \frac{640}{R_V \times C_V} \text{ (approx.)}, \text{ where}$$

f is in Hz, R in $\text{k}\Omega$ and C in μF .

The 'External VCO Control voltage' (U_V), applied to pin 19, determines the duty-cycle of the square-wave output of the VCO. This, in turn, varies the harmonic content (the 'sound'), producing an effect somewhat similar to that of a voltage controlled filter. The duty-cycle can be calculated from

$$\text{duty-cycle} = \frac{U_V}{U_V + U_2} \times 50\% \text{ (approx.)}.$$

A 50% duty-cycle can therefore be obtained by simply connecting pin 19 to pin 16, provided the pitch control input is enabled (pin 22 at logic 0). However, a 50% duty-cycle can also be obtained by holding pin 19 at logic 1 (+5 V), even when the VCO is controlled by the SLF.

Noise generator

A clock generator, 'Noise Clock', drives the noise generator. The external resistor, R_E , sets an internal current level; the value of this resistor should be approximately 39 to 47 $\text{k}\Omega$. The noise generator proper is a pseudorandom white noise generator (see Elektor E 21, January 1977). Its noise output is satisfactory for most audio applications, but in some cases a signal containing more low-frequency components may be desired. This can be achieved by applying a TTL-compatible squarewave of a suitable frequency to the 'External Noise Clock' input (pin 3).

The output from the noise generator is fed to a low-pass filter ('Noise Filter'). The cut-off frequency ($f_{-3\text{dB}}$) of this filter is determined by the values of R_N and C_N :

$$f_{-3\text{dB}} = \frac{1280}{R_N \times C_N} \text{ (approx.)}, \text{ where}$$

f is in Hz, R in $\text{k}\Omega$ and C in μF .

Mixer

One or more of the signals from the SLF oscillator, VCO and Noise generator are selected and mixed in the mixer stage. The choice of signals is determined by the logic levels at the 'mixer select' inputs (pins 25, 26, 27), as shown in table 1. Note that, although it would appear logical to have each of the three 'mixer select' inputs correspond to one of the three possible signals, this is not in fact the case.

The output from the mixer is fed to an 'Envelope Generator/Modulator', which will be described furtheron.

System enable and one-shot

The audio output from the IC is only enabled when a logic '0' is applied to the 'System Enable' input (pin B). No audio output is produced if a logic '1' is applied to this pin. The System Enable logic also triggers a monostable multivibrator (one-shot) on the negative-going edge of the system enable signal at pin 9. The latter signal should remain at logic 0 for the full duration of the one-shot period. The one-shot is intended mainly for obtaining momentary sounds, such as gunshots, bells, etc. The maximum length of the one-shot period (T) is 10 seconds, and is determined by the values of R_T and C_T as follows:

$$T = 0.8 \times R_T \times C_T \text{ (approx.)}, \text{ where}$$

T is in seconds, R in $\text{M}\Omega$ and C in μF .

It is also possible to connect an external one-shot (or timer), for instance if a longer period is required. In this case R_T and C_T are omitted. Initially pin 23 is held at logic 0 and the pulse is started by applying a negative-going edge to pin 9; the pulse is terminated by taking pin 23 to logic 1.

Envelope

The output signal from the mixer is fed to the 'Envelope Generator/Modulator'. Basically, of course, envelope shaping is equivalent to amplitude modulation, and the modulating signal in this case is determined by the logic levels at the two 'Envelope Select' inputs (pins 1 and 28) as shown in table 2.

The wave-shapes shown in table 2 are given as examples to illustrate the various types of envelope shaping. In these examples, the mixer output is shown as a pseudo-random binary noise signal as produced by the noise generator.

The envelope shown for the one-shot requires some further explanation. In general, the audio signal will not be turned on end off instantaneously; the gradual rise to full output level ('attack') and gradual level reduction at the end of the pulse ('decay') are both determined in part by the value of the capacitor (C_B) connected to pin B. In combination with this capacitor, R_E (pin 10) sets the attack time T_A and R_D (pin 20) the decay time:

$$T_A = R_E \times C_B \text{ (approx.)}$$

$$T_D = R_D \times C_B \text{ (approx.)}, \text{ where}$$

T is in seconds, R in $\text{M}\Omega$ and C in μF .

Output amplifier

The gain of the output amplifier A is set by the values of resistors R_F and R_G . Since the signal level applied to this amplifier is constant, it is more practical to specify the peak audio output level ($U_{O,PEAK}$) as a function of these resistors:

$$U_{O,PEAK} = 3.4 \frac{R_F}{R_G} \text{ (approx.)}, \text{ where}$$

u is in volts and R in $\text{k}\Omega$.

To avoid clipping, the peak output level should be less than 1.2 V, which means that R_G should be at least three times the value of R_F .

Final note

If some sections of the IC are not used in a particular application, the corresponding external components may be omitted. For instance, if the noise generator is not required, R_E , R_N and C_N may be omitted and pins 4, 5 and 6 are left floating.

Table 3 lists the most important operating characteristics. A few typical applications are shown in figure 2.

Texas Instruments preliminary data sheet.

Figure 1. Internal block diagram of the 'complex sound generator', type SN76477N. The external resistors and capacitors shown will not be required for all applications.

Figure 2. Typical applications of the SN76477N. The sound effects generated are those for a train or propeller aircraft (2a), a gunshot or explosion (2b) and various siren and science fiction effects (2c).

APPLIKATOR

Table 1

mixer select			mixer output
C (pin 27)	B (pin 26)	A (pin 25)	
0	0	0	VCO
0	0	1	noise
0	1	0	SLF
0	1	1	VCO/noise
1	0	0	SLF/noise
1	0	1	SLF/VCO
1	1	0	SLF/VCO/noise
1	1	1	

Table 2

mixer			
		VCO	one shot
envelope select	modulation	envelope modulator output	
A (pin 28)	B (pin 28)	VCO/AM	
0	0	no modulation	
1	0	one shot	
1	1	VCO/product	

Table 3

Absolute maximum ratings

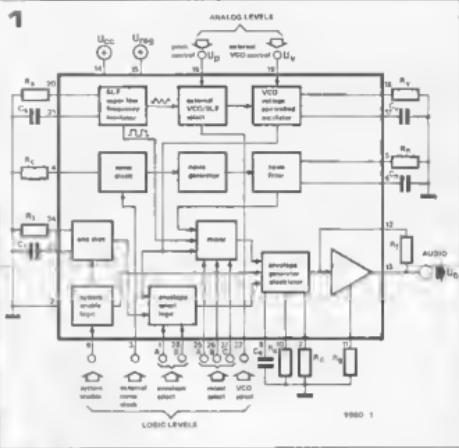
supply voltage U_{reg} (pin 15)	6	V
supply voltage U_{cc} (pin 14)	12	V
input voltage at any other pin	6	V

Recommended operating conditions

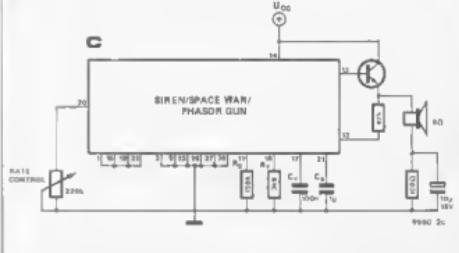
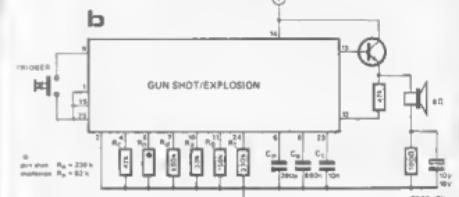
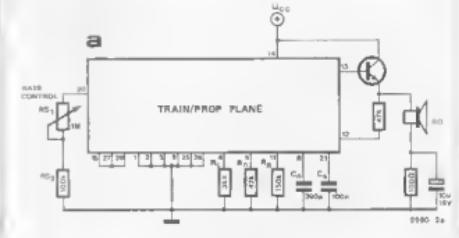
	min	typ	max	
supply voltage U_{reg} (pin 15)	4.5	5.0	5.5	V
supply voltage U_{cc} (pin 14)	7.5	9.0	10	V
operating temperature	0	25	70	°C

Operating characteristics ($U_{reg} = 5$ V; $T_{amb} = 25^\circ\text{C}$)

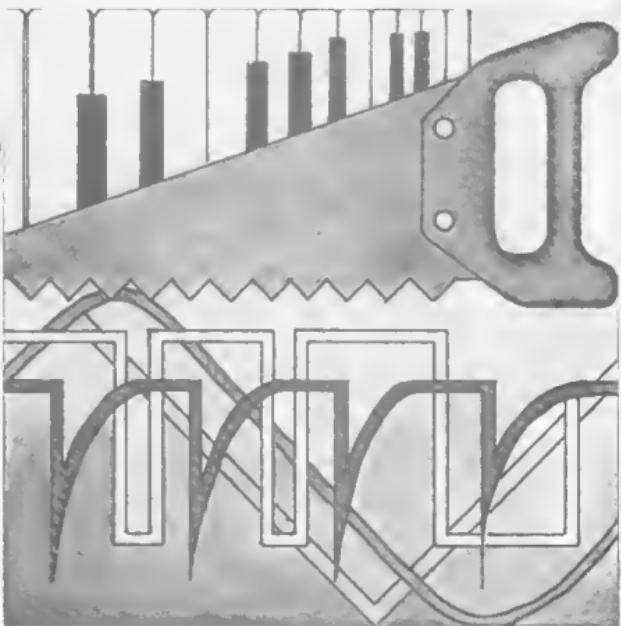
	min	typ	max	
supply current I_{cc} (no ext. load)				
U_{reg} ($U_{cc} = 8.25$ V, $I_{load} = 10$ mA)	4.5	15	40	mA
input regulation for U_{reg}				
current through resistors	1	150	200	μA
logic '1' input current,				
system enable input				
other inputs				
logic '1' input voltage	2.0	40	100	μA
logic '0' input voltage				
VCO cut-off (pin 16)	2.5	52	55	μA
maximum output voltage				
swing, peak-to-peak	2.5	0.8	0.9	V
output impedance				
	2.5	100	100	Ω



2



24 dB- VCF



In response to requests from readers who have built the Formant synthesiser the following article presents a design for a voltage-controlled filter whose slope is considerably steeper than that of the original VCF, in fact 24 dB/octave as opposed to 12 dB/octave. The filter offers a choice of highpass or lowpass modes and slopes of 6, 12, 18 or 24 dB/octave.

VCFs with an extremely steep slope seem to have a particular appeal for most synthesiser enthusiasts because of the greater range of tonal possibilities that they offer. Formant users are evidently no exception to this rule judging by the number of requests for a 24 dB/octave VCF. Of course, the filter described here is not restricted to use with the Formant synthesiser, but may also be used with other synthesiser designs.

New possibilities

It should be stated at the outset that the 24 dB VCF does not render the existing 12 dB design obsolete. On the contrary, the two filters are complementary to one another and can be used in combination to provide greatly increased possibilities for tailoring the harmonic structure of the sounds produced by Formant.

For example, the 12 dB VCF can be used in the bandpass mode together with the steep filtering of the 24 dB VCF to produce selective tone coloration. The two filters can be controlled by the same envelope shaper or by different envelope shapers, and may be connected in cascade or in parallel. The latter arrangement offers several interesting possibilities. For example, hard, metallic sounds can be produced by applying a short, steep envelope voltage to the 12 dB VCF and a longer, shallower contour to the 24 dB VCF.

If the filter inputs are connected in parallel then interesting effects may be obtained by connecting one VCF output to one input of a stereo amplifier

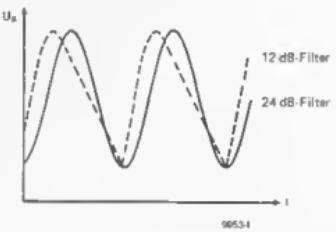
and the other VCF output to the other input. This gives rise to a very distinctive dynamic amplitude characteristic and stereo imaging, particularly if the two VCFs are controlled by different envelope shapers.

The audible differences between the 12 dB VCF and the 24 dB VCF are quite prominent. The 12 dB VCF produces sounds that are distinctly 'electronic', which can have a slightly fatiguing effect on the listener during extended playing sessions. The sounds produced by the 24 dB VCF, on the other hand, are much more 'natural', and can be listened to for extended periods without fatigue. This effect is probably due to the more severe filtering of higher harmonics which the 24 dB VCF provides when used in the lowpass mode, since these harmonics tend to make the sound of the 12 dB VCF much more shrill than that of the 24 dB VCF.

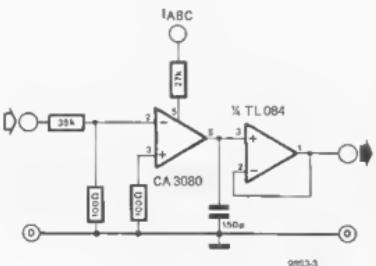
The effect of the steeper filter slope of the 24 dB VCF is illustrated in figure 1, which shows the different outputs from the 12 dB VCF (dotted line) and 24 dB VCF (continuous line) when fed with a sawtooth waveform. It is apparent that, due to the almost complete removal of the harmonics of the sawtooth, the output of the 24 dB VCF is practically a sinewave, whereas the original waveform is still apparent at the output of the 12 dB VCF since the harmonics are only partially removed.

It is clear from the foregoing that a 24 dB VCF greatly extends the musical possibilities of a synthesiser and is virtually a must for the serious user.

1



2



Design of the 24 dB VCF

Most 24 dB VCFs are variations on the heavily-patented design by R.A. Moog, which has been around for a number of years. However, thanks to the advent of inexpensive IC OTAs (Operational Transconductance Amplifiers) a more versatile design than Moog's is now possible, which can be operated in highpass or lowpass modes with slopes of 6, 12, 18 or 24 dB/octave. Even greater slopes than 24 dB would be possible, but experiments have shown that a greater slope does not result in a corresponding increase in tonal quality.

The design of the basic filter section shown in figure 2 is very similar to that of the 12 dB VCF, which was described in detail on page 12-29 of Elektor 31, December 1977. However, advantage has been taken of recent developments in FET op-amp technology to simplify the design. As described in that article the basic filter section is an integrator or 6 dB/octave lowpass section consisting of an OTA driving a capacitor. The voltage/current transconductance (g_m) of the OTA can be varied by an external control current and hence, via an exponential voltage/current converter, from an external control voltage. This control current alters the time constant of the integrator and hence the turnover frequency of the filter section.

The output current of the OTA must all flow into the capacitor, otherwise the integrator characteristic will be less than ideal. This means that the output of the OTA must be buffered by an amplifier with a high input impedance.

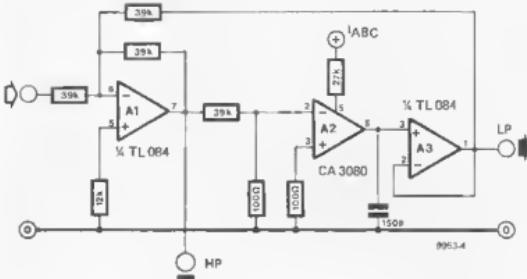
Figure 1. This illustrates the difference between the outputs of a 12 dB/octave VCF and a 24 dB/octave VCF having the same turnover frequency, when fed with a sawtooth input. The 24 dB VCF removes practically all the harmonics giving a sinewave output, whereas the original waveshape is still distinguishable at the output of the 12 dB VCF.

Figure 2. The basic filter section of the 24 dB VCF is the same as that of the 12 dB VCF, i.e. an OTA integrator followed by a FET op-amp buffer.

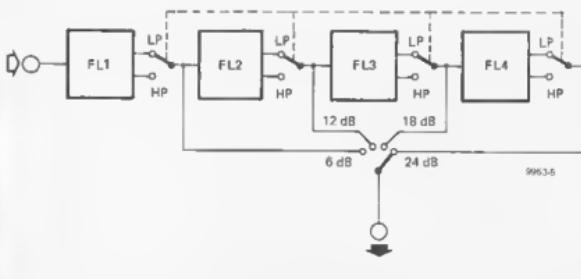
Figure 3. The highpass function is obtained by connecting the 6 dB lowpass section in the feedback loop of an operational amplifier.

Figure 4. To obtain a 24 dB/octave filter, four 6 dB/octave sections are cascaded.

3



4



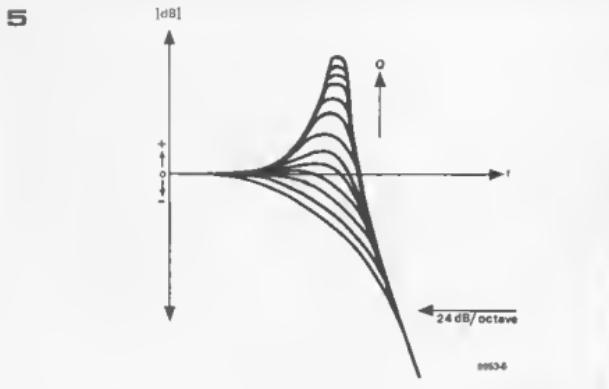
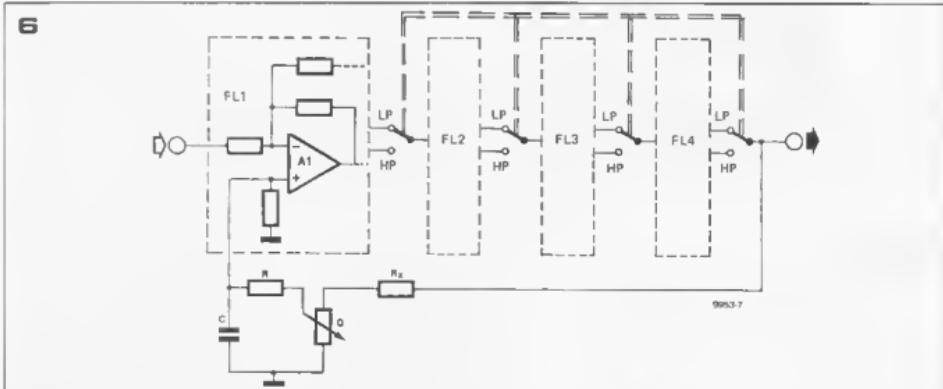


Figure 5. Positive feedback around the entire filter allows the response to be boosted about the turnover frequency. The degree of boost can be varied by a 'Q' control.

Figure 6. Block diagram of the 24 dB/octave filter, showing how the Q control is incorporated.

Figure 7. Complete circuit of the 24 dB VCF. The exponential voltage/current converter is identical to that used in the 12 dB VCF.



12 dB VCF this was achieved by using a discrete FET source follower and a 741 op-amp. Fortunately, relatively inexpensive quad FET op-amps such as the Texas TL084 are now available. The use of one of these ICs greatly simplifies the design and obviates the need to select FETs, which is rather a chore when one considers that the 24 dB VCF uses four integrator stages.

Highpass function

The highpass mode of the filter is achieved by connecting the 6 dB/octave lowpass section in the negative feedback loop of an operational amplifier, A1, as shown in figure 3. A highpass filter response is then available at the output of A1 whilst a lowpass response is simultaneously available at the output of A3. Of course, this arrangement gives only a 6 dB/octave slope per section, and in order to obtain a 24 dB/octave filter four filter sections, built according to the circuit of figure 3, must be cascaded as shown in figure 4. Switching at the output of each section allows selection of highpass or lowpass mode, whilst a 4-position switch allows 1, 2, 3, or 4 filter sections to be switched in to give 6-, 12-, 18-, or 24 dB/octave slopes

respectively.

It is apparent that this arrangement is different from the two-integrator loop or state-variable filter which formed the basis of the 12 dB/octave filter. In the 12 dB/octave filter, lowpass, highpass, bandpass and notch modes were available simultaneously at various points in the circuit, though in fact only one function at a time could be selected at the output.

An interesting effect, shown in figure 5, can be obtained with the 24 dB VCF if a feedback loop is connected from the output of the cascaded filters to the non-inverting input of the first stage as illustrated in figure 6. Due to the phase shift around the turnover frequency this causes positive feedback, which boosts the gain of the filter around the turnover frequency as shown in figure 5. The degree of boost is adjustable by means of a 'Q' control. The choice of R_X is important as too much feedback would cause the circuit to oscillate, so the value of R_X is a compromise between stability and a reasonable degree of boost.

Complete circuit

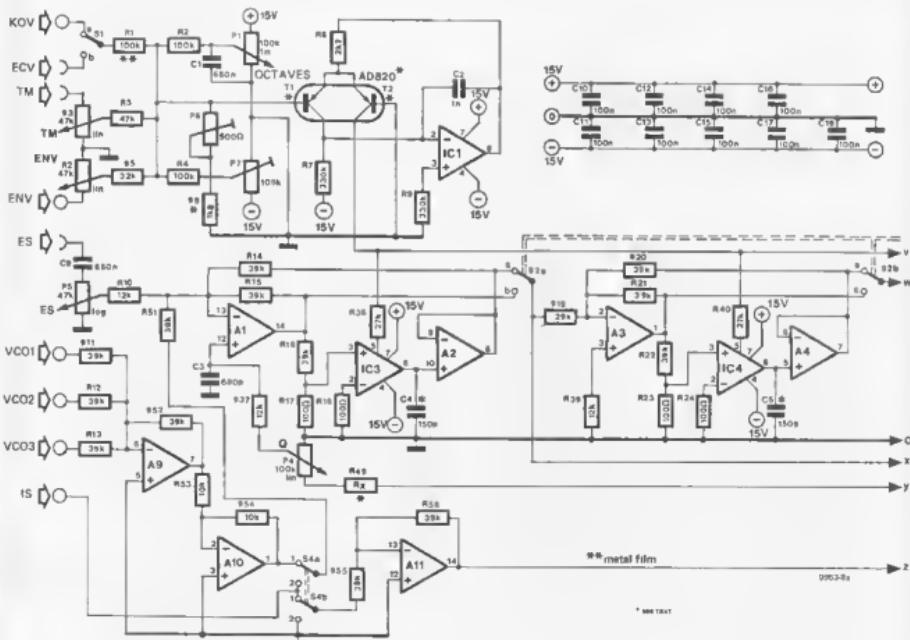
The complete circuit of the 24 dB VCE

is given in figure 7. The exponential converter, constructed around T_1 , T_2 and $IC1_1$, is identical to that used in the 12 dB VCF and gives the same 1 octave per volt characteristic to the turnover frequency of the filter. The control voltage inputs are also the same as for the 12 dB VCF, and are listed in table I. Since the 24 dB VCF must have the option of being connected in parallel or in cascade with the 12 dB VCF, the input switching arrangements are a little complicated. $A9$ and $A10$ form a non-inverting summing amplifier for the three VCO inputs, whilst the output of the 12 dB VCF is fed in via the IS connection. With $S4$ in position 2 the output of $A10$ is disconnected, so the VCO inputs are inhibited. The output of the 12 dB VCF is fed to the input of the 24 dB VCF via $S4$ and $R51$, so that the two VCFs are in cascade.

With S4 in position I the output of A10 is connected to the inputs of the 24 dB VCF, whilst the output of the 12 dB VCF is routed through A11. The output of A11 and the output of the 24 dB VCF are added together in the output summing amplifier A12, i.e. the two MCs are integrated in parallel.

The four 6 dB/octave filter sections

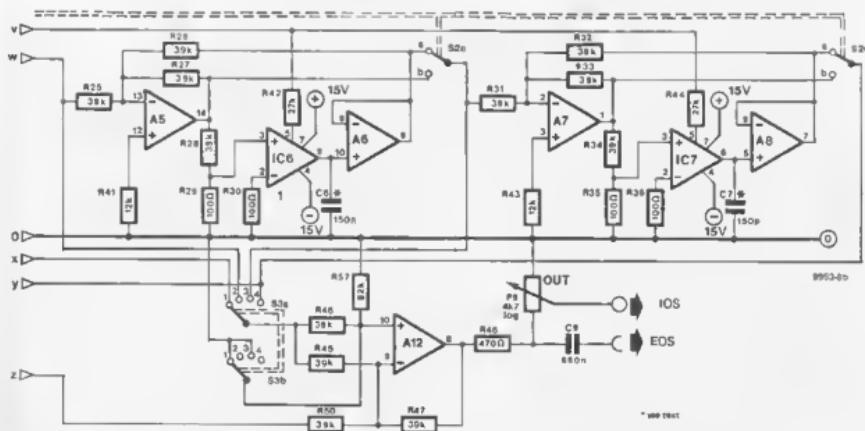
7a



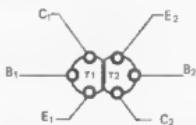
7b

$$A1 + A2 + A3 + A4 = IC2 = TL084$$

IC1 = μ A 741 Minidip
IC3 = CA 3080*
IC4 = CA 3080*
IC6 = CA 3080*
IC7 = CA 3080*



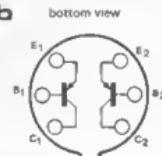
8a



bottom view

9953-9a

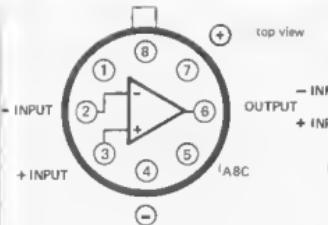
8b



9953-9b

BFX 11
BFX36
2N3808 . . . 2N38011
AD 820 . . . 822

8c



CA3080(A)

top view

INPUT

+ INPUT

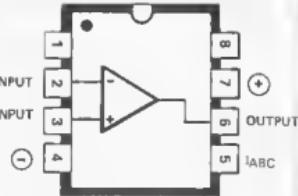
INPUT

OUTPUT

+ INPUT

INPUT

-



9953-9c

comprise A1 to A8 and IC3 to IC7. The four poles of switch S2 select between highpass and lowpass modes, while S3 selects the filter output and hence the slope. The reason that S3 is a two-pole switch may not be immediately apparent, but is easily explained. Ignoring the phase shift introduced by the action of the filter, i.e. considering only signals in the filter passband, each filter section inverts the signal fed to it, since A1, A3, A5 and A7 are connected as inverting amplifiers. This means that the outputs of alternate filter sections are either in phase or inverted with respect to the input signal. To ensure that the filter output is in the same phase relationship to the input signal whatever filter slope is selected, S3b is arranged to switch A12 between the inverting and non-inverting modes to cancel the inversions produced by the filter sections.

Like the 12 dB VCF, the 24 dB VCF has two outputs, a hardware output connection IOS and an uncommitted output, EOS, which is connected to a front panel socket.

Construction

As far as the choice of components for the 24 dB VCF goes, the same general comments apply that were made about the 12 dB VCF and the Formant synthesiser in general. All components should be of the highest quality; resistors should be 5% carbon film types except where metal oxide or metal film types are specified; capacitors should preferably be polyester, polystyrene or polycarbonate, and must be these types where specified. Semiconductors should be from a reputable manufacturer. As with the 12 dB VCF the dual transistor may be any of the types specified in

Figure 8. Pinouts for the dual transistors and CA3080.

Figure 9. Printed circuit board and component layout for the 24 dB VCF. (EPS 9953-1).

Table 1. Summary of the control functions and input/output connections of the 24 dB VCF.

Table 1

a) hardware inputs (not on the front panel)	
KDV	= Keyboard Output Voltage (from interface receiver)
ENV	= Envelope shaper Control Voltage (from ADSR unit)
VCO 1,2,3	= Signals from VCDs 1, 2, 3
IS	= Internal signal from the 12 dB VCF
b) external inputs (sockets on front panel)	
ECV	= External Control Voltage (for exponential generator of the VCF)
TM	= Tone Colour Modulation Input
ES	= External Signal (from e.g. noise module)
c) outputs	
IDS	= Internal Output Signal (from VCF to VCA)
EDS	= External Output Signal (socket on front panel)
d) controls	
TM	= P3: sets tone colour modulation level
ES	= P5: sets external signal level
ENV	= P2: sets envelope shaper control voltage
DCTAVES	= P1: coarse frequency adjustment
D	= P4: sets level of peak boost around turnover frequency
DUT	= P6: sets IDS output level
e) switches	
ECV/KOV	= S1: selects external or internal control voltage input

Parts list to figures 8 and 10

Resistors:

R1 = 100 k metal oxide
R2, R4 = 100 k
R3 = 47 k
R5 = 33 k
R6 = 1 k
R7, R9 = 330 k
R8 = 2 k
R10, R37, R39, R41, R43 = 12 k
R11 . . . R16, R19 . . . R22,
R25 . . . R28, R31 . . . R34, R45,
R46, R47, R50, R51, R52, R55,
R56 = 39 k
R17, R18, R23, R24, R29, R30,
R35, R36 = 100 Ω
R38, R40, R42, R44 = 27 k
R48 = 470 Ω
R49 = 100 k (see text)
R53, R54 = 10 k
R57 = 82 k

Potentiometer:

P1, P4 = 100 k linear
P2, P3 = 47 k (50 k) linear
P5 = 47 k (50 k) logarithmic
P6 = 4.7 k (5 k) logarithmic
P7 = 100 k preset
P8 = 470 Ω (500 Ω) preset

Capacitors:

C1, C8, C9 = 680 n
C2 = 1 n
C3 = 680 p (polystyrene, not
ceramic)
C4, C5, C6, C7 = 150 p
(polystyrene, not ceramic)
C10 . . . C18 = 100 n

Semiconductors:

IC1 = 741
IC2, IC5 = TL 084, TL 074
IC8 = TL 084, TL 074, LM 324
IC3 . . . IC6 = CA 3080,
CA 3080A (MINIDIP or TO;
see text)
T1, T2 = AD 820 . . . 822,
2N3808 . . . 3811, 8FX 11,
8FX 36 (see text) or
2 x 8C5578

Miscellaneous:

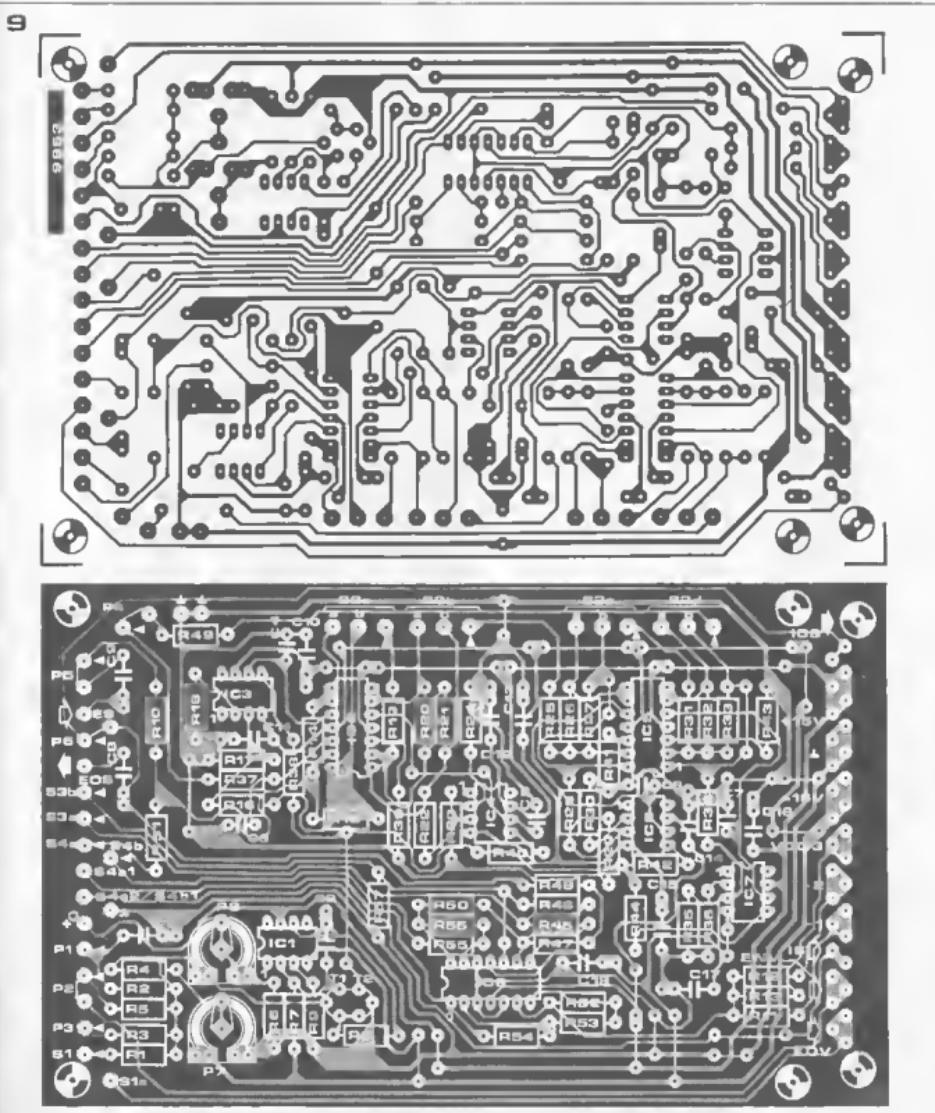
31-pin DIN 41617 connector or
terminal pins
S1 = SPDT
S2 = 4-pole double throw
S3 = 2-pole 4-way; index angle
approx. 30°
S4 = DPDT
4 miniature sockets, 3.5 mm dia.
7 . 13 . . . 15 mm collet knobs
with pointer (to match existing
synthesiser modules).

the parts list, or may be home-made by gluing together two normal transistors, though in this case thermal tracking will not be quite so good. The CA3080 should preferably be in a MINIDIP package to fit the hole spacings on the p.c. board, though the metal can type can be made to fit by splaying the leads. The pinouts for the dual transistors and the CA3080 are given in figure 8.

Although not absolutely necessary, it is a good idea to select OTA's with approximately the same transconductance.

since the four sections of the filter will then have almost the same turnover frequency. The CA3080 is available in two versions, the standard version, in which the ratio between the maximum and minimum g_m is 2:1, and the CA3080A, in which the spread in g_m is only 1.6:1. A test circuit and test procedure for selecting ICs with similar g_m are given at the end of the article, and it is certainly worthwhile buying a few extra OTAs and selecting the four with the most similar g_m . The 'reject' devices are per-

flectly acceptable for use in the 12 dB VCF or VCA, and need not be wasted. The other ICs in the circuit should all be TL074 or TL084 quad BIFET op-amps, although for IC8 it is only permissible to use an LM324. Thanks to the use of quad op-amps it is possible to accommodate the 24 dB VCF on a standard Eurocard-size (160 mm x 100 mm) p.c. board, although the control connections are not all on the front edge of the board. The printed circuit pattern and component layout for this board are



given in figure 9, while a front panel layout is given in figure 10.

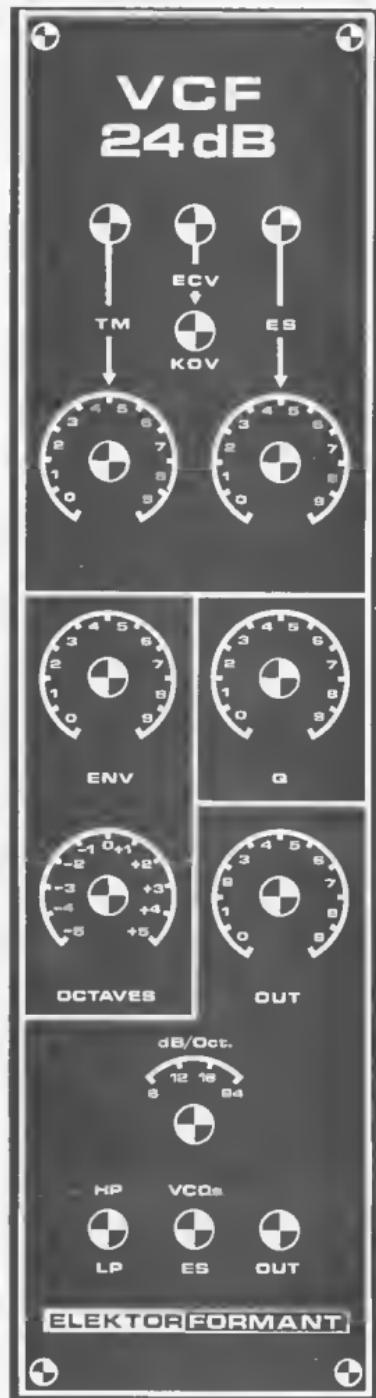
10

Test and adjustment

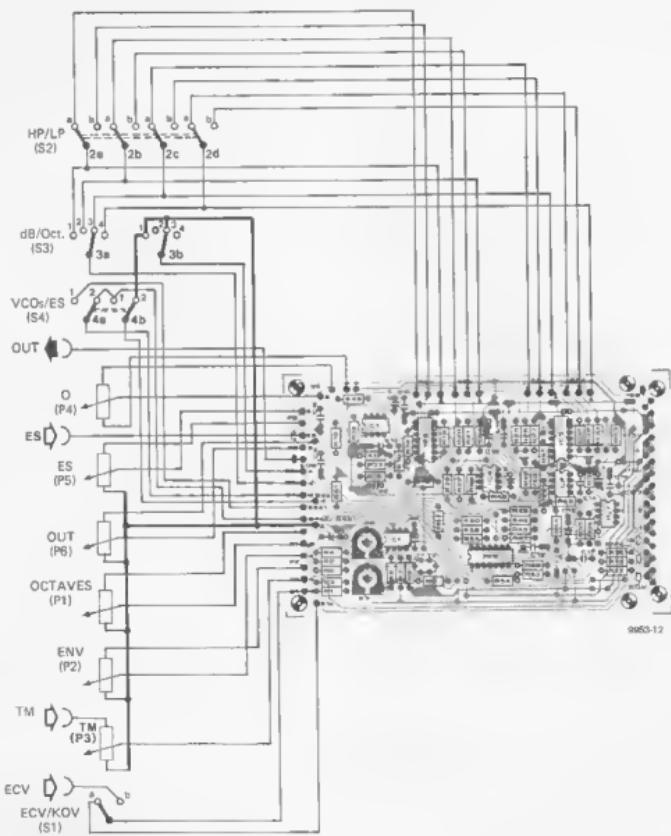
To enable the exponential converter and the filter section to be tested separately they are joined by a wire link which runs across the board from T2 to a point adjacent to R15. This link should be omitted until the VCF has been tested.

To test the filter section it is necessary to provide a temporary control current. This is done by connecting a 100 k log potentiometer between -15 V and ground, with its wiper linked to the junction of R39 and R4 via a multimeter set to the $100\text{ }\mu\text{A}$ DC range. The test then proceeds as follows:

1. Turn the wiper of P4 fully towards ground, select 24 dB slope with S3 and adjust the control current to $100\text{ }\mu\text{A}$.
2. Feed a sinewave signal into the ES socket and adjust either the sinewave amplitude or PS for 2.5 V peak-to-peak measured on a oscilloscope at the wiper of P5.
3. Monitor the filter output on the 'scope and check the operation of the filter by varying the sinewave frequency and checking that the signal is attenuated above the turnover frequency in the lowpass mode and below the turnover frequency in the highpass mode.
4. The function of S3 should now be checked. Set S3 to the 6 dB position and S2 to the LP position. Increase the frequency of the input signal until the output of the filter is 6 dB down on (i.e. 50% of) what it was in the passband where the response was level. Now switch to 12 dB, 18 dB and 24 dB and check that the response is respectively 12, 18 and 24 dB down, i.e. is reduced to 25%, 12.5% and 6.25% of its original value. The exact results of this test will depend upon the matching of the OTAs.
5. Set the Q control, P4, to its maximum value, when the circuit should show no sign of oscillation. If the circuit does oscillate it will be necessary to increase the value R49. If it does not oscillate then the Q range can be increased by decreasing R49, taking care that instability does not occur.
6. Finally, the linearity of the turnover frequency v. control current characteristic should be checked. Adjust the input frequency until the response is a convenient number of dB down (say 6 dB). Double the control current then double the input frequency and the response should still be 6 dB down.
7. To check the exponential converter connect a 27 k resistor in series with a multimeter set to the $100\text{ }\mu\text{A}$ range between the collector of T2 and the -15 V rail. Then follow the test



11



12

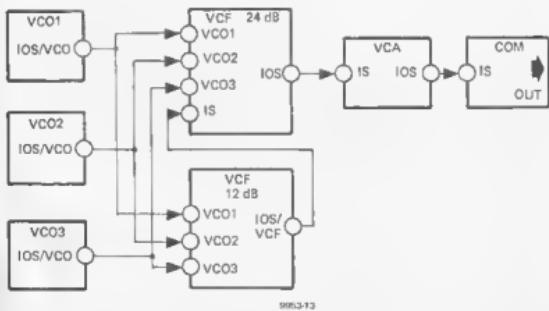


Figure 10. Front panel layout for the VCF. (EPS 9953-2).

Figure 11. Showing the wiring between the p.c. board and the front-panel mounted components.

Figure 12. The 24 dB VCF is connected into the Forment system between the 12 dB VCF and the VCA.

Figure 13. Test circuit for the selection of DTAs.

procedure given on page 12-33 of Elektor 32, column I line 51. The offset and octaves per volt adjustments can also be carried out using the procedure given in this issue. During the offset adjustment P4 should be set to minimum and S3 should be set to the 24 dB position. During the octaves/volt adjustment of P8 the Q control, P4, should be set to maximum, as with the 12 dB VCF.

Using the 24 dB VCF

Before the 24 dB VCF can be put to work it must first be connected into the Formant system. Fortunately, as far as the signal paths go this involves changing only two connections and adding three more. As can be seen from figure 12, the 24 dB VCF is connected between the 12 dB VCF and the VCA, so that the IOS output of the 12 dB VCF now goes to the IS input of the 24 dB VCF instead of to the VCA, whilst the VCA receives its input from the IOS output of the 24 dB VCF. The 24 dB VCF also has inputs from the three VCOs.

In addition to the signal connections the 24 dB VCF must also be provided with supply to the VCF module in accordance with the standard practice for Formant. Provision of control voltage inputs from the ADSR envelope shapers will be discussed later.

For satisfactory operation of the 24 dB VCF the correct setting of the input level is important, even more than in the case of the 12 dB VCF. On the one hand, the distortion level should not be so large that distortion occurs, but on the other hand it should not be so small that the signal-to-noise ratio is degraded. The 24 dB VCF is designed so that the optimum input level is obtained using three VCOs set to maximum output.

with one waveform selected per VCO. If more than three VCOs are in use or more than one output waveform is selected from each VCO then the VCO output levels must be reduced. On the other hand, if only one VCO is used then the signal level may be too low. In this case it is best to patch the EOS socket of the VCO to the ES input of the VCF, since this input has approximately three times the sensitivity of the hardwired VCO inputs.

The 24 dB VCF is capable of the same basic functions as the 12 dB VCF; driven by the KOV control voltage it will operate as a tracking filter, whilst the ENV and TM inputs allow dynamic modulation of the harmonic content of the VCF output. Due to the greater slope of the 24 dB VCF the setting of the ENV level control is more critical than with the 12 dB VCF, but if correctly adjusted then subtle nuances in the tonal character of the output signal are possible.

The question arises as to which ADSR envelope shaper should be used to control the 24 dB VCF, since only two are built into the basic Formant system, and control the VCA and 12 dB VCF respectively. Because of the modular construction of Formant it is, of course, perfectly feasible to build a third envelope shaper, which is the most versatile arrangement. The alternatives are to patch one of the other ADSR outputs to the TM input of the 24 dB VCF, or to hardwire the ENV input of the 24 dB VCF to the output of the envelope shaper that controls the 12 dB VCF. This latter arrangement is probably preferable, as it allows the ADSR signal to be fed to one or both VCFs by suitable adjustment of their ENV controls and also allows the possibility of patching the output of the other envelope shaper into the TM input of either VCF.

Appendix

OTA selection procedure

Although not absolutely essential, it is well worth selecting OTAs with closely matched transconductance characteristics to ensure that the four filter sections track accurately.

A test circuit for the OTAs is given in figure 13. This should be fed with a sinewave signal of about 2 V peak-to-peak (or 0.7 V measured on an AC voltmeter) from a signal generator or from one of the VCOs. The output should be monitored on a 'scope or AC voltmeter. With a control current of $100\ \mu\text{A}$, measured on the multimeter in series with R_5 , the output voltage should be between 0.7 V and 1.3 V peak-to-peak. Without changing the input level or control current the OTAs to be tested should be plugged into the circuit one at a time and the output level for each OTA noted. The four OTAs whose output levels are most similar should be used in the VCF. The circuit can also be used to check the linearity of the transconductance v. control current characteristic of the OTAs, e.g. doubling the control current should double the output of the test circuit and halving the control current should halve the output.

buffered/unbuffered CMOS

The two most popular logic families are TTL (Transistor-Transistor Logic) and CMOS (Complementary Metal-Oxide Semiconductor). TTL is based on bipolar transistors, i.e. transistors whose operation depends upon two types of charge carriers, electrons and holes (e.g. normal NPN and PNP transistors).

Other logic families based on bipolar technology include DTL (Diode-Transistor Logic), RTL (Resistor-Transistor Logic), HLL (High-Level Logic), ECL (Emitter-Coupled Logic), DCTL (Direct-Coupled Transistor Logic) and I^2L (Integrated Injection Logic). With the exception of ECL for high-speed circuits, these other logic families are rarely used by the home constructor, although I^2L is a developing new technology which is beginning to offer serious competition both to TTL and CMOS.

CMOS logic ICs, on the other hand, are based on FET (Field Effect Transistor) technology, sometimes known as unipolar devices because their operation depends upon only one type of charge carrier. The FETs used in CMOS are of the insulated-gate or MOSFET type, so called because the gate connection is insulated from the silicon substrate of the device by a layer of silicon dioxide. This means that MOSFETs have an extremely high input resistance, which is something of a mixed blessing, as will be seen later.

TTL v. CMOS

Although a host of logic devices are available in both TTL and CMOS, ranging from the simple to the very complex, a look at the internal circuit of one device from both families will serve to illustrate the differences between them. Figure 1a shows the circuit of a TTL two-input NOR gate, whilst figure 1b shows the internal circuit of a CMOS two-input NOR-gate (unbuffered type).

The TTL NOR gate operates in the following manner: if either one or both of the inputs to the gate is high (or floating) then base current will flow into T2 or T3 (or both) through the 4k resistors and the forward-biased base-collector junction of T1 or T4. T2 and/or T3 will thus be turned on and current

Many CMOS digital ICs are now available in two versions, buffered and unbuffered. The lack of information available to the amateur on the differences between them has given rise to some confusion as to the compatibility of the two types. This article examines both types of CMOS, compares them with the other popular logic family, TTL, and indicates the applications in which buffered CMOS is superior to unbuffered, and vice versa.

will flow through the 1k resistor, turning on T6. Due to the forward voltage of D1 and the saturation voltage of T6 the emitter of T5 is at a higher potential than the base, so T5 is turned off. The output of the gate is thus low, the output voltage being equal to the saturation voltage of T6.

When both inputs to the gate are low then both T1 and T4 will be turned on by current flowing through the 4k resistors into their bases. The bases of T2 and T3 will be pulled low by T1 and T4 respectively, so these transistors will be turned off. T5 will thus be turned on by current flowing into its base via the 1k6 resistor, while T6 will be turned off. The output of the gate will thus be high, the output voltage (with no load) being supply voltage minus the base-emitter voltage of T5 and the forward voltage of D1.

Whereas the TTL gate uses only one type of bipolar transistor (NPN) the CMOS gate uses complementary pairs of P-channel and N-channel MOSFETs, hence the term *Complementary Metal Oxide Semiconductor*.

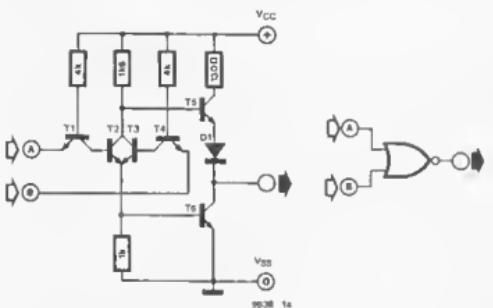
The basic configuration of the CMOS two-input NOR gate shown in figure 1b is simply two complementary pairs of MOSFETs. The diodes and resistors at the two inputs are protection circuits, which are required only at external inputs to the gate. In more complex logic devices where some elements of the circuit have no external connections these protection circuits would be omitted, only being included in sections of the circuit connected to the pins of the IC. This simple gate configuration allows CMOS IC chips to have a much greater packing density than TTL devices, since the resistors used in TTL circuits occupy a large proportion of the chip area.

Operation of the CMOS NOR gate is quite easy to understand. When both inputs are low then the P-channel FETs T1 and T2, which are connected in series, are both turned on, whilst the N-channel FETs T3 and T4 are both turned off.

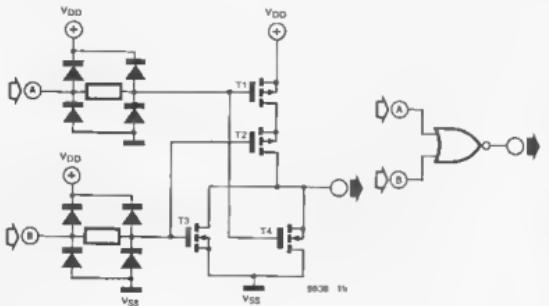
The output of the gate is therefore high, being connected to positive supply via the drain-source resistances of T1 and T2. Under no-load conditions the high



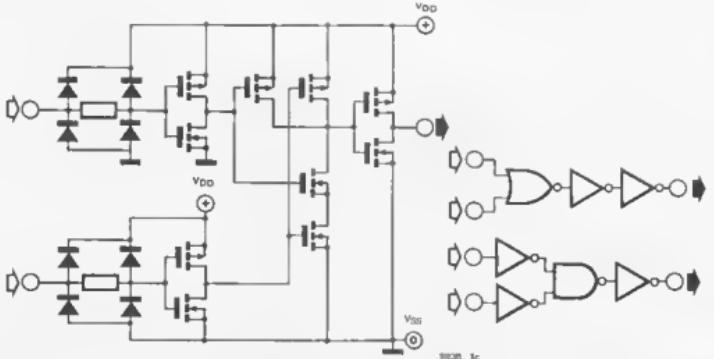
1a



1b



1c



output voltage is virtually equal to supply voltage (V_{DD}).

If either input to the gate is low then T1 or T2 (or both) will be turned off, effectively disconnecting the output from positive supply. T3 or T4 will be turned on, so the output will be pulled low via the drain-source resistance of one (or both) of these transistors. Under no-load conditions the low output voltage will be virtually zero (V_{SS}). The characteristics of CMOS circuits approach those of an 'ideal' logic family much more closely than TTL, for a number of reasons.

1. An ideal logic family should be capable of operating over a wide range of supply voltages. CMOS can operate over a wide supply range, but TTL is limited to a small operating range around 5 V, due to the use of resistors and semiconductor junction voltage drops to define operating conditions within the circuit.
2. The transfer characteristics (i.e. output voltage plotted against input voltage) of a logic gate should approach that of an ideal electronic switch, i.e. for input voltages up to half supply the output should remain in one state, above half supply the output should be in the opposite state, the transition from one state to the other being as abrupt as possible. This is illustrated in figure 2, which compares an ideal transfer characteristic with those of TTL and CMOS. It can be seen that CMOS approaches the ideal much more closely than TTL, which has a decidedly asymmetric transfer characteristic.
3. The output of an ideal logic device should be capable of driving the inputs of a large number of similar devices (fanout capability) without the load causing the output voltage to fall below its permissible high level or rise above its permissible low level. The low output of a TTL device connected to the input of another TTL device must be able to sink the current of around 1.6 mA which

flows out of the emitter of the input transistor. In the high state the base-emitter junction of the input transistor is reverse-biased, so a high output needs to supply very little current. Most TTL devices, except buffers, can drive 10 other TTL devices (quoted as a fanout of 10).

CMOS, on the other hand, has a virtually unlimited fanout, at any rate for low operating speeds. Since the input resistance of a CMOS gate is practically infinite it imposes no DC loading on the output of the gate which is driving it. As the operating speed increases, however, the picture changes. The input of a CMOS gate has a capacitance of typically 5 pF due to the capacitor formed by the gate electrodes, oxide layer and substrate. In addition the circuitry external to the device will have its own stray capacitances. The output of a CMOS gate has a resistance of several hundred ohms which forms a lowpass filter with these stray capacitances. This limits the maximum operating frequency so that a trade-off must be made between output drive capability and operating speed. Increased load capacitance also increases the power dissipation of CMOS.

4. The power consumption of an ideal logic family should be as low as possible. TTL devices rely on the various resistors in the circuit to charge and discharge the transistor capacitances. These RC time constants determine the maximum operating speed of TTL, so the resistor values cannot be too large or speed performance will suffer. Furthermore, since several of the transistors in a TTL gate are turned on at any time, providing a path to ground via these resistors, TTL circuits dissipate a considerable amount of power. In addition to the standard (74XX series) TTL circuits there are other variants of TTL which reflect the speed/dissipation trade-off. Low-

Figures 1a. Internal circuit of a two-input TTL NOR gate.

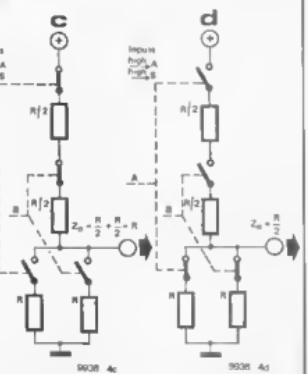
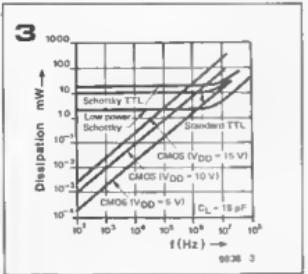
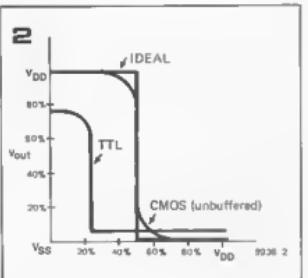
b. Internal circuit of an unbuffered CMOS two-input NOR gate.

c. Internal circuit of a buffered CMOS two-input NOR gate.

Figure 2. Comparison of the transfer characteristics of TTL and unbuffered CMOS.

Figure 3. Power dissipation (per gate) versus frequency for standard TTL, Schottky TTL, low-power Schottky TTL and CMOS.

Figure 4. Illustrating that the output resistance of buffered CMOS remains constant, whilst that of unbuffered CMOS depends on how many inputs of a gate are used.



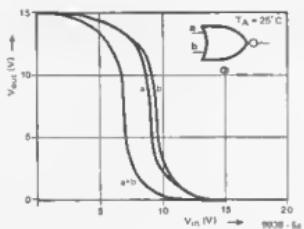
power TTL, for example, uses higher resistance values, giving lower dissipation at the expense of speed. High-speed TTL uses lower resistance values, increasing operating speed at the expense of dissipation. Schottky TTL utilises Schottky barrier transistors to obtain high operating speeds with dissipation similar to that of standard TTL, while low-power Schottky TTL uses Schottky transistors and higher resistance values to obtain the same speed as standard TTL but with reduced dissipation. It seems fairly likely that low-power Schottky will eventually become the standard TTL logic family.

However, returning to CMOS circuits, it is fairly apparent that the static dissipation of these devices is virtually zero. Since the upper and lower transistors of a complementary pair cannot be turned on simultaneously there is never a current path to ground, and since the input resistance of a CMOS gate is extremely large no current is taken by the inputs of other gates which are being driven.

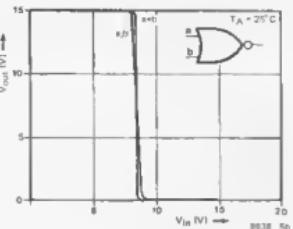
The situation is different for AC operation, however. As the output of a CMOS gate switches between its high and low states it passes through a transitional region where both FETs of a complementary pair are turned on. This causes a current of several millamps to flow from the supply rail to ground through the two FETs, causing power to be dissipated in them. At low operating speeds, provided the input pulses fed to the gate have short risetimes, the average power dissipation will be small since both FETs are on for only a very small proportion of the total time. As the input frequency increases, however, the transition region will occupy a greater proportion of the total cycle and the power dissipation will increase. A similar effect occurs in TTL due to both output transistors being turned on simultaneously, but at low operating speeds it is the static power consumption which is predominant. This is illustrated in figure 3, which shows power consumption per gate versus frequency for CMOS, standard TTL, Schottky TTL and low-power Schottky TTL. It can be seen that the power consumption of CMOS rises steadily with frequency, whereas that of TTL stays fairly constant up to about 5 MHz.

5. An ideal logic family should have good noise immunity. The definitions of noise immunity are quite complicated, but basically it is the ability of a logic device to resist false switching by noise pulses. The so-called DC noise immunity of CMOS is typically 45% of supply voltage, with 20% being guaranteed. TTL, on the other hand, has a DC noise immunity of only 400 mV or so. The one par-

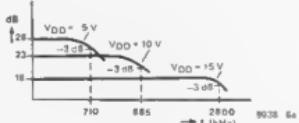
5a



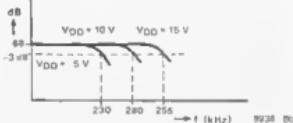
b



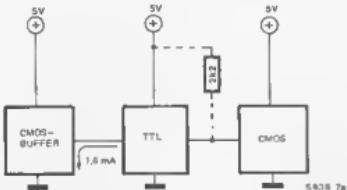
6a



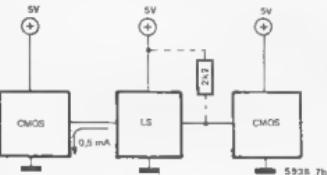
b



7a



b



parameter in which TTL scores over CMOS is operating speed, the propagation delay of a TTL gate being of the 10 ns, whilst that of unbuffered CMOS is an order of 10 greater. Buffered CMOS is even slower.

Unbuffered v. buffered CMOS

All the foregoing comments apply to unbuffered CMOS devices, and the differences between these and buffered devices will now be considered. Figure 1c shows the internal circuit of a buffered, two-input CMOS NOR gate. In fact, this NOR gate actually consists of a NAND gate with inverters on its inputs and output, which (by DeMorgan's theorem) is logically equivalent to a NOR function. An alternative approach, adopted by some manufacturers, is to use a NOR gate whose output is buffered by two cascaded inverters. The logic diagrams for both these arrangements are shown in figure 1c. Both are logically equivalent to a single NOR gate. The buffered NOR gate is obviously much more complex than the unbuffered gate, so what advantage does it offer, and what are its disadvantages?

To begin with, since the output of a buffer gate consists of a single, complementary pair, a buffered gate has a constant output resistance, equal to the drain-source resistance of whichever FET is switched on. This means that the rise and fall times of the output signal are fixed for given load conditions, which can be an important factor in some applications. This is illustrated in figure 4a, in which the output FETs of a buffered gate are represented as two switches and two series resistors.

The output resistance of an unbuffered gate, on the other hand, depends on the state of the inputs. This is illustrated in figures 4b to 4d, in which a two input unbuffered NOR gate is represented by switches and resistors. If one input of the gate is high the output is low, the output resistance being the drain-source resistance of one of the lower FETs. If both inputs are low then the output is high and the output resistance is that of the two upper FETs connected in series. However, if both inputs are high then both lower FETs are turned on and the output resistance is the parallel connection of the drain source resistances of the two FETs, i.e. $R/2$. With multi-input gates the variation in output resistance

can be even greater. This variation in output resistance also affects the transfer characteristics as will be seen later.

Gain

Since a buffered CMOS gate has two extra stages compared with an unbuffered gate it has a much higher gain, which is reflected in the transfer characteristics. Figure 5a shows the transfer characteristics of an unbuffered two-input NOR gate whilst figure 5b shows the transfer characteristics of a buffered gate. Not only are the buffered gate much closer to the ideal, due to the high gain, but it makes little difference whether one or both inputs are used, due to a combination of the higher gain and constant output resistance. With the unbuffered gate, on the other hand, there is a marked difference between using one input and using both inputs. The gain of buffered CMOS is also practically independent of supply voltage, whereas that of unbuffered CMOS is extremely voltage dependent. This is illustrated in figures 6a and 6b which show the gain of unbuffered and buffered

Table 1

	buffered	unbuffered
propagation delay	150	60 ns
noise immunity	30	20% of V_{DD}
noise margin	1	0.5 V
output impedance (four- input gate)	400	100 .. 400 Ω
transition time	100	50 .. 100 ns
AC gain	68	23 dB
bandwidth	280	885 kHz
output oscillation (determined experimentally)	can occur with input signals \geq 1 ms	undetectable for inputs \leq 100 ms
input capacitance	1 .. 2	2 .. 3 pF
average	2 .. 4	5 .. 10 pF
maximum		

measured for ± 5 V supply and $C_L = 50$ pF

Table 2

Application	Buffered	Unbuffered
High-speed	*	*
low-speed in high noise environments	*	*
low-speed signals with slow edges	*	*
applications requiring constant output resistance, e.g. D/A, A/D conversion	*	*
linear amplification, medium gain at high frequencies		*
linear amplification, high gain at low frequencies	*	*

CMOS, versus frequency, at three different supply voltages. A further advantage of the greater gain of buffered CMOS is that noise immunity is improved due to the better transfer characteristics. The final advantage of buffered CMOS is that it has a lower input capacitance than unbuffered CMOS.

Disadvantages

Buffered CMOS is not without its disadvantages, however. Since a buffered gate has more stages than an unbuffered gate it has an inherently greater propagation delay, which means that its maximum operating speed is lower. Secondly, due to their higher gain, buffered CMOS gates have a tendency to oscillate as the output passes through the transition region if the risetime of the input signal is fairly slow. This means that buffered gates are less suitable for low-speed systems where the pulses have slow edges. It also means that buffered gates are less suitable for linear applications, where the input is biased so that the output is at half supply. Here again oscillation is likely to occur since the output of the gate is in its transition region.

Clearly, buffered and unbuffered CMOS devices are not always interchangeable, so in order to help readers choose the best device for a particular application tables 1 and 2 are given. Table 1 lists the principal differences between buffered and unbuffered devices, whilst table 2 indicates which type of device is preferred for particular applications.

CMOS-TTL-CMOS

It is sometimes necessary to interface CMOS circuits to TTL circuits, and this can be done in a number of ways. To drive standard TTL a current sink capability of 1.6 mA per TTL input is required. A normal CMOS output can sink only 0.5 mA, so to drive standard TTL a CMOS buffer such as the 4049 (inverting) or 4050 (non-inverting) must be used. Two TTL loads can be driven with one of these devices. Driving CMOS from TTL presents little difficulty due to the greater source/sink capability of TTL. The only minor problem is that the 'high' output voltage of TTL may be inadequate to drive CMOS, so a pullup resistor is connected from the output of the TTL gate to positive supply. This ensures that the

high output of the TTL gate is equal to supply voltage and therefore adequate to drive CMOS. Interfacing CMOS to standard TTL is illustrated in figure 7a. CMOS can be interfaced to low-power TTL and low-power Schottky TTL without difficulty, since all CMOS ICs which conform to the JEDEC norm can directly drive one low-power (Schottky) TTL load. Low-power (Schottky) TTL can, of course, drive CMOS directly if a pullup resistor is included. This is illustrated in figure 7b.

B-series CMOS

To add another confusion factor to the CMOS scene, not only are CMOS ICs available in buffered and unbuffered types, but there are also two different series of CMOS. Prior to 1976 many manufacturers produced 'A' series CMOS, a principal parameter of which was an absolute maximum supply voltage of 15 V, although some manufacturers produced devices capable of withstanding 18 V.

A-series CMOS ICs were available mainly in unbuffered versions, though

Figure 5. Comparison of the transfer characteristics of unbuffered CMOS and buffered CMOS.

Figure 6. Comparison of the gain of unbuffered CMOS with that of buffered CMOS.

Figure 7. Interfacing CMOS to standard TTL and low-power (Schottky) TTL.

Table 1. Comparison of the principal specifications of buffered and unbuffered CMOS.

Table 2. Applications preference table for buffered and unbuffered CMOS.

Table 3. Main points of the JEDEC specification for B-series CMOS.

Table 3

JEDEC B	
Absolute Maximum Ratings (Voltages referenced to V _{SS}):	
DC Supply Voltage	-0.5 to +18 V
Input Voltage	-0.5 to V_{DD} + 0.5 V
DC Input Current (any one input)	± 10 mA
Storage Temperature Range	-65 to +150°C
Total dissipation	400 mW
Recommended Operating Conditions:	
DC Supply Voltage	+3 to +15 V
Operating-Temperature Range:	
Military-Range Devices	-55 to +125°C
Commercial-Range Devices	-40 to +85°C

8



RCA
CD4007AE
349

Figure 8. Markings on CMOS ICs from RCA, who prefix their 4000 type numbers with the letters 'CD'. The suffix is either 'A' for A-series (unbuffered), 'UB' for B-series unbuffered and 'B' for B-series buffered, followed by 'E' to indicate a plastic package or 'O' to indicate a ceramic package.

10



MC14021B
A77-25

Figure 10. Motorola CMOS ICs. Prefix 'MC'. Note that Motorola use '14000' type numbers instead of 4000, but apart from the extra '1' their type numbers correspond to those of other manufacturers. Pre-JEDEC-B Motorola ICs carry the suffix 'A' for devices with a maximum rating of 18 V and 'C' for devices with a maximum rating of 16 V. Package suffix is 'P' for plastic and 'L' for ceramic.

12



74164
74164-1
NS/18
CD4066CN
MM5660X

Figure 12. National Semiconductors CMOS ICs. Note the two different vignettes used by this company. The 4000 type number is prefixed 'CD'. Suffix is 'B' for B-series buffered, 'UB' for B-series unbuffered. A-series devices have no special suffix. This is followed by a letter to indicate the temperature range of the device ('C' for standard, 'M' for extended), and the last letter of the suffix is the package code, 'N' for plastic and 'D' or 'J' for ceramic. National devices also carry an 'MM 5000' type number which is peculiar to National. In addition to 4000-series CMOS National also make a series of CMOS which is pin compatible with 74XX-series TTL and is called the 74C-series.

9



Figure 8. Solid State Scientific CMOS IC. Prefix 'SCL', suffix 'A' for A-series unbuffered, 'A/B' for A-series buffered, 'UB' for B-series unbuffered and 'B' for B-series buffered. This is followed by 'E' for plastic package or 'D' for ceramic package. Maximum supply voltage of all SSS CMOS ICs is 18 V.

11



CD4040AE/TP4040AN
N 7628

Figure 11. Texas Instruments CMOS IC. This IC carries two type numbers! One type number prefixed 'CD' is identical to that used by RCA, the other is prefixed 'TP'. Suffix 'A' for A-series unbuffered or 'B' for B-series buffered. Package suffix is 'N' for plastic or 'J' for ceramic.

13



F 4511PC
7704
INDONESIA

Figure 13. A Fairchild CMOS IC. Type numbers of Fairchild CMOS devices are prefixed by 'F' and sometimes by '3'. All Fairchild ICs are buffered except where the circuit configuration makes this impossible. Package suffix 'P' for plastic or 'D' for ceramic, followed by 'C' for commercial temperature range or 'M' for military temperature range.

some buffered versions were produced. A-series CMOS has now largely been replaced by 'B' series, though there are still considerable numbers of A-series devices around, particularly on the amateur market.

In 1976 the major CMOS manufacturers met to draw up a standard for B-series CMOS, a major feature of which is an absolute maximum supply voltage of 18 V (though some manufacturers quote 20 V for their devices) and a maximum recommended operating voltage of 15 V.

The principal specifications of the JEDEC standard for B-series CMOS are given in table 3. B-series devices are available in both buffered and unbuffered versions, except where the internal circuit of the device makes buffered or unbuffered operation mandatory.

Identification marks

The problem faced by the average

constructor, going into a shop to buy a CMOS IC, is finding out if a device is A-series or B-series, buffered or unbuffered. This is not helped by the fact that many retailers know even less than the purchaser, added to which different manufacturers each have their own code for marking devices.

The usual procedure is that the package is printed with the CMOS 4000-series type number of the device, which has a prefix peculiar to the manufacturer and a suffix which indicates if the device is

14



Figure 14. A Philips/Velvo CMOS IC. Philips ICs are prefixed 'HEF' and suffixed 'B' for buffered or 'UB' for unbuffered. Some Philips ICs have the suffix 'V' which denotes that the recommended maximum operating voltage is only 12.5 V, and that the device is buffered. The last letter of the suffix is 'P' for plastic package or 'D' for ceramic package.

15



Figure 15. All the S's. The foregoing list of manufacturers is by no means comprehensive, and Signetics, Silex, SGS-ATES, Siltat and Solitron could be added, to name just those manufacturers whose names begin with S. However, the exemplars given should help the reader to know what to look for in IC markings. Note that the remarks made about package suffixes apply only to dual-in-line (DIL) packages. Flatpacks, rarely used by the home constructor, have different suffixes.

As a final note, different manufacturers have different ways of indicating the orientation of an IC. Most use a notch in the end of the IC adjacent to pin 1; some use a dot, bump or figure 1 on the top of the package next to pin 1.



A- or B-series, buffered or unbuffered. The suffix is usually A for A-series unbuffered, A/B for A-series buffered, UB for B-series unbuffered and B for B-series buffered. The suffix may also contain other letters which give additional information such as the type of package. However, this is by no means a general rule, and the only way to be certain is to be familiar with the codes used by different manufacturers. Identifying the manufacturer of an IC is in itself no mean feat, as manufacturers do not print their full name but just the initial letters, or else some form of symbol or vignette. Figures 8 to 15 show some typical CMOS ICs from the major manufacturers. An explanation of the markings on each IC is given in the caption to each figure.

Using CMOS ICs

For low and medium speed applications CMOS is an almost ideal logic family, as it offers the advantages already discussed, i.e. low static power consumption, high noise immunity, wide range of operating voltages and large fanout. However, it does suffer from one major disadvantage, susceptibility to damage by static charge. The oxide layer which separates the gate electrodes from the substrate is extremely thin (typically 1000 Å) and has a breakdown voltage between 80 and 120 volts. The human body can become charged to several

kilovolts simply by walking across a nylon carpet, and though the energy stored is very low due to the small capacitance (around 300 pF) of the body, it is still sufficient to break down the oxide layer, which has an extremely high resistance and very small capacitance.

Unlike the breakdown of a reverse-biased PN junction, breakdown of a MOSFET gate is irreversible, since a small hole is actually punched through the oxide layer by the discharge. Fortunately the manufacturers of CMOS ICs do incorporate input protection circuits. These usually take the form of pairs of diodes connected between the inputs and supply lines, together with series resistors to limit the current. In the event of a voltage exceeding positive supply being applied to the input the upper diode is forward biased and the current is shunted away to the low impedance of the positive supply rail. For negative input voltages the lower diode is reverse-biased and the current is shunted away to ground. Of course, this protection is really effective only if the device is in circuit with the power applied. When handling CMOS devices suitable precautions must still be taken and even when a device is in circuit signals should never be applied to the inputs with the power switched off. Unlike TTL, the unused inputs of a CMOS device must not be left floating, as the output of the device may then be in its transition state (around half

supply voltage) in which a large current is drawn. Unused inputs must always be connected to positive supply (VDD) or the zero volt rail (VSS).

To summarise, the following precautions should be taken when using CMOS:

1. Store CMOS ICs with their pins embedded in conductive plastic foam or aluminium foil - not in expanded polystyrene (which practice is not unknown).
2. Don't handle CMOS ICs any more than necessary.
3. Work on a metal surface, such as a tin tray or aluminium foil, earthed through a 1M resistor (A 1M resistor will leak away static charges, but in the event of simultaneous contact with mains live and the work surface the current flow will be insufficient to give the constructor a shock).
4. Before handling CMOS ICs, always earth yourself to the work surface. If you leave the workbench for any reason, earth yourself upon returning.
5. Use an earthed soldering iron.
6. Connect unused inputs of CMOS devices to VDD or VSS.
7. Don't apply signals to the inputs of CMOS gates if power to the circuit is switched off.

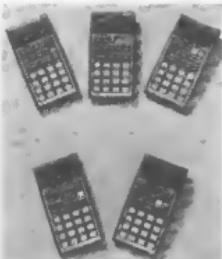
Literature

RCA Application note ICAN 6558.
Data books from the major CMOS manufacturers.

market

New calculators

A new series of five financial and scientific calculators featuring an advanced degree of human engineering was announced today by the Hewlett-Packard Company. Prices for the new Series E calculators fall comfortably within reach of students and younger professional and business people. Calculators in the new range are the HP-37E business management, HP-38E advanced financial



programmable, the HP-31E scientific, HP-32E advanced scientific and HP-33E programmable scientific models. All feature more powerful, larger, easier-to-read displays, diagnostic error code systems, accuracies previously available only in the most advanced calculators, non-slip rubber base pads, and positive click-action keys.

HP, Ltd., King Street Lane, Winnersh, Wokingham, Berkshire, RG11 5AR England.

(827 M)

Compact lab. supply

A new low-cost, three-in-one bench Power Supply from Hewlett-Packard is designed for engineers who design and test breadboards and prototypes using integrated circuits. The compact HP Model 6235A Triple-output Power Supply delivers three adjustable DC output voltages: 0 to 6 V at 1 A, 0 to +18 V at 0.2 A and 0 to -18 V at 0.2 A. A single 0 to 36 V output at 0.2 A

can also be obtained by connecting across the -18 V and +18 V terminals.

The controls, meter, and binding posts are all arranged conveniently on the front panel. One voltage control simultaneously adjusts the +18 V and -18 V outputs, which track one another to power operational amplifiers and other circuits requiring balanced positive and negative voltages. The supply's dual outputs have added versatility with an adjustable tracking ratio control that can set the negative output to a lower voltage than that of the positive output. Once the tracking ratio control has been set by the user, the voltage ratio between the positive and negative outputs remains constant as the +18 V voltage control varies both outputs. A separate voltage control sets the 0 to +6 V output. The supply is of the constant voltage/current limit type with each output voltage being continuously adjustable over its range, while the maximum current available is limited automatically to prevent overloading. The unit's outputs share a common output terminal and are isolated from chassis ground so that any output terminal can be grounded if desired. Voltage or current can be selected and monitored quickly for each output with pushbutton

meter switches. With dimensions of only 90 mm high, 155 mm wide, and 190 mm deep, the new supply is small enough to be picked up with one hand and takes up a minimum of bench space. The HP6235A weighs only 2.3 kg. It can be powered from 115 V or 230 V, 47-63 Hz AC input.

Hewlett-Packard Limited, King Street Lane, Winnersh, Wokingham, Berkshire. RG11 5AR England. (828 M)

20 MHz scope

The Leader LBO-508 is a dual-trace oscilloscope with bandwidth of 20 MHz and sensitivity of 10 mV/cm. Stabilized power supplies ensure a measuring accuracy of $\pm 3\%$, and the display screen is 8 x 10 cms. Fixed and variable controls cover a sensitivity of 10 mV/cm to 50 V/cm, and with an add function and CH.2 trace invert, inputs may be added or subtracted. Triggering may be selected from CH.1 or CH.2 and



the circuit will extract sync signals from both T.V. line and frame signals. Timebase from 0.5 μ s/cm-0.2 sec/cm also has a variable control and X 5 magnification. AUTO/NORMAL triggering is provided, as is an external trigger input. An X-Y function switches one input to the horizontal axis for X-Y display.

Martron Ltd., 20 Park St., Princes Risborough, Bucks, England.

(830 M)

1 W audio amp

Recently added to the range of Sprague low to medium power audio devices, is the ULN-2283B integrated audio power amplifier. Its predominant features are the wide operating voltage range and low quiescent current drain. A minimum number of external parts, together with 'on-chip' short-circuit protection, enhance the system's reliability. The wide operating voltage range



makes this device eminently suitable for use in hand-held battery-operated equipment. In an environment, where space is at a premium, an important feature is the fact that this circuit does not require a heat-sink, as the copper-alloy lead frame conducts the heat into the printed wiring board.

Sprague Benelux, Industriezone, P.O. Box 104, 9600 Ronse, Belgium.

(832 M)

Low power IF/AF circuit for fm receivers

Plessey Semiconductors new SL1664 circuit offers the entire IF and audio sections of an FM receiver, including a 250 mW output stage, in a single integrated circuit. It may be used with IF's between 455 kHz and 21.4 MHz and will give super signal/noise ratio with low deviations and high IF's, as well as low distortion with high deviation and low IF.

The SL1664 has a sensitivity of 10 microvolts or better, and a standby consumption of 20 mW, making it ideal for both low-power pocket receivers for broadcast FM and portable narrow FM transceivers.

The device incorporates a stable squelch system and operates from supplies of between +6 and +9 volts. Its operating temperature range is -30° to +70° C and it is supplied in an 18 lead plastic DIL package. The SL1664 was designed to use external LC quadrature circuitry which means that even in high performance receivers for narrow deviation signals of 1.5 kHz or less, simple quadrature circuitry will give excellent S/N ratio and expensive crystal quadrature circuitry is not necessary.

Plessey Semiconductors, Cheney Manor, Swindon, Wiltshire SN2 2QW, England.

(837 M)



